

Chip cooling with integrated carbon nanotube microfin architectures

K. Kordás, G. Tóth, P. Moilanen, M. Kumpumäki, J. Vähäkangas, and A. Uusimäki
*Microelectronics and Materials Physics Laboratories, Department of Electrical and Information Engineering,
 University of Oulu, P.O. Box 4500, FIN-90014 Oulu, Finland and EMPART Research Group of
 Infotech Oulu, University of Oulu, P.O. Box 4500, FIN-90014 Oulu, Finland*

R. Vajtai^{a)} and P. M. Ajayan

*Department of Materials Science and Engineering, Rensselaer Polytechnic Institute, Troy, New York 12180
 and Rensselaer Nanotechnology Center, Rensselaer Polytechnic Institute, Troy, New York 12180*

(Received 15 January 2007; accepted 9 February 2007; published online 20 March 2007)

Efficient cooling of silicon chips using microfin structures made of aligned multiwalled carbon nanotube arrays is achieved. The tiny cooling elements mounted on the back side of the chips enable power dissipation from the heated chips on the level of modern electronics demands. The nanotube fins are mechanically superior compared to other materials being ten times lighter, flexible, and stiff at the same time. These properties accompanied with the relative simplicity of the fabrication makes the nanotube structures strong candidates for future on-chip thermal management applications.

© 2007 American Institute of Physics. [DOI: 10.1063/1.2714281]

High power consumption and the corresponding problem of heat dissipation are two of the most serious limitations in high performance electronics today. Several solutions for component thermal management have been suggested,^{1–4} but there is a continuous need for developing cooling methods and utilizing previously not tested materials to be able to dissipate heat in a more efficient manner. Superior thermal conductivity of carbon nanotubes (CNTs) (Ref. 5) has prompted suggestions of their applications in thermal management of high power electronics. This thermal conductivity advantage of carbon nanotubes over other materials has been exploited mainly in improving the thermal conductivity of nanotube-polymer composites, namely, embedding nanotubes randomly in polymer matrices to reach enhanced thermal conductivity.^{6–8} Recently a microchannel liquid cooler structure equipped with arrays of carbon nanotubes was reported, where using water-flow cooling, a moderate of $\sim 15 \text{ W cm}^{-2}$ enhancement of heat dissipation was obtained.^{9,10}

In this work, we demonstrate a simple and scalable nanotube-on-chip assembly, using a unique processing and transfer technique to integrate nanotube structures on the chip, where the advantageous mechanical and thermal properties of carbon nanotubes are exploited to remove heat from silicon chip components. For a 1 mm^2 surface area test chip the applied power can be $\sim 1 \text{ W}$ larger when a carbon nanotube cooler is applied—compared to the case of the bare chip—to reach the same temperature. The cooling performance of the nanotube fin structures accompanied with their low weight, mechanical robustness, and ease of fabrication make them candidates for on-chip thermal management applications.

Thick films consisting of $\sim 1.2 \text{ mm}$ long aligned multiwalled carbon nanotubes grown on Si/SiO₂ templates from a xylene/ferrocene precursor^{11–13} by catalytic chemical vapor deposition deposited at $770 \text{ }^\circ\text{C}$ were used in our experiments (Fig. 1). The diameters of nanotubes in the films show a broad distribution of 10–90 nm [Fig. 1(c)]. After detaching

the nanotube layers from the templates, structures of 10×10 fin array blocks were fabricated in the freestanding films by laser-assisted surface patterning [Figs. 1(a) and 1(b)] with a defocused ($\sim 800 \text{ }\mu\text{m}$ offset, spot diameter in the focal plane of $\sim 15 \text{ }\mu\text{m}$) 3ω Nd:YVO₄ pulsed laser having a pulse duration of 20 ns, repetition rate of 90 kHz, average power of 300 mW, and scan rate of 50 mm/s with 15 scan repetitions. Each cooling element of nanotube fin arrays has a size of $\sim 1.2 \times 1.0 \times 1.0 \text{ mm}^3$ and a mass of $\sim 0.27 \text{ mg}$.

The structure designed to test the CNT fin structures consists of a thermometer flip chip mounted on a customized silicon substrate, and the array of the fin block itself being soldered onto the back side of the flip chip (Fig. 2). First, the flip chips were mounted on the substrate, then the CNT blocks were positioned and soldered on the chips (see supplementary movie, Ref. 14). To be able to solder the bottom of the CNT cooler blocks on the back side of the chips, both surfaces were cleaned and sputtered up with a thin $\sim 50 \text{ nm}$ layer of chromium (adhesion promoter) and subsequently with a solderable copper film of $\sim 2 \text{ }\mu\text{m}$ average thickness. Owing to the individual and collective mechanical strengths¹⁵ in spite of the severe mechanical load conditions

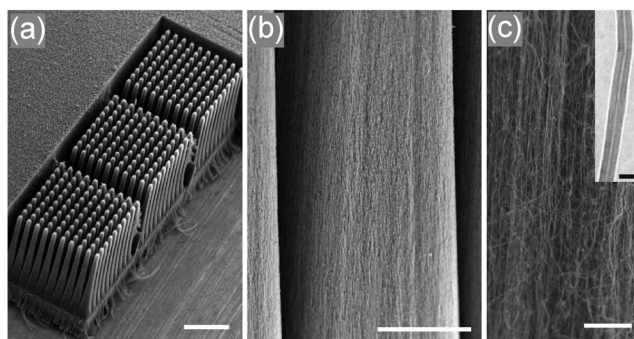


FIG. 1. Morphology and structure of laser-patterned CNT films. (a) Microstructure of three cooler blocks laser etched next to each other in the CNT film (scale bar: $500 \text{ }\mu\text{m}$). (b) Grooves and a pyramidal fin obelisk of aligned nanotubes (scale bar: $50 \text{ }\mu\text{m}$). (c) Close-up image of the aligned nanotubes (scale bar: $5 \text{ }\mu\text{m}$). The inset in the figure shows an energy filtered electron microscopy image of a well-graphitized nanotube (scale bar: 50 nm).

^{a)}Electronic mail: vajtai@rpi.edu

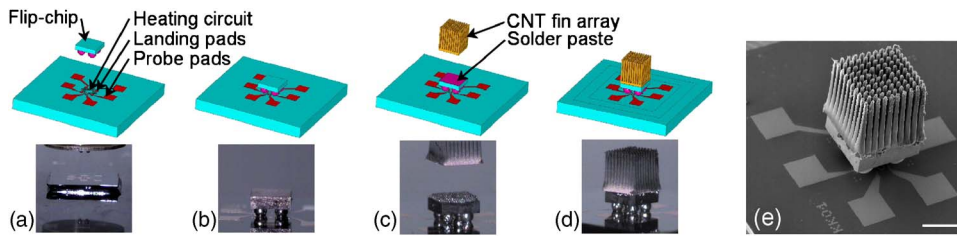


FIG. 2. (Color online) Phases of substrate/flip-chip/CNT-cooler assembling (see supporting Movie, Ref. 14). (a) Positioning and (b) soldering the flip chip on the Cu landing pads of the substrate (this structure also served as a reference). (c) Solder paste dispensing, CNT array positioning, and (d) soldering on the Cu coated backside of the chip. (e) Field emission scanning electron microscopy image of an assembled structure (scale bar: 500 μm).

during the assembly and testing phases of the experiments, no any damage or degradation of the nanotube films was observed proving the robustness and feasibility of CNT cooler structures for practical applications. The assembly was measured on a probe station to record the chip temperature versus heating power characteristics under various thermal loads (up to ~ 7 W) and cooling gas flow rates (N_2 at 0 – 2 l min^{-1}) with a flow perpendicular to the upper facet of the chip. The temperature of the heated chips is extracted from the output of the thermometer chips. Reference measurements were done without the nanotube fins, but otherwise under the same conditions.

In the measurements, the Joule heat generated on the substrate by the heating circuit to increase the temperature of the thermometer chip was dissipated by the nanotube-on-chip assembly, resulting in a decreased chip temperature as compared to the corresponding chip without the cooling block (Fig. 3). Using natural convection, 11% more power is observed to be dissipated from the chip that has the attached nanotube fin structures; i.e., 31.9 mW K^{-1} power was dissipated instead of 28.8 mW K^{-1} [Fig. 3(a)]. Under forced N_2 flow the cooling performance with the fins is improved by 19%; i.e., 82.8 mW K^{-1} of power could be dissipated instead of 69.8 mW K^{-1} . These results mean that applying the nanotube fin structure would allow the dissipation of ~ 30 and ~ 100 W cm^{-2} more power at 100 $^\circ\text{C}$ from a hot chip for the cases of natural and forced convections, respectively. As the carbon nanotube arrays form low density structures,¹⁶ the extra power dissipated per weight of the added structure can be estimated as high as 1.1 or 3.7 kW g^{-1} for these two cases studied, as calculated for the corresponding geometry using a measured density of the nanotube films, ~ 0.35 g cm^{-3} . These numbers demonstrate the possibility of a light-weight solid state add-on structure for an on-chip thermal management scheme, which works without involving complex fluid flow procedures for heat removal.

To compare the cooling performance with other materials, finned copper structures were fabricated and mounted on test chips. The measured temperature versus power curves show very similar results for the two materials, i.e., copper and nanotubes perform fairly equally. In other experiments, measurements carried out on contiguous CNT blocks without etching the fin structure showed poor cooling performance. The densely populated forest of nanotubes ($\sim 10^2$ μm^{-2}) hampered the flow of N_2 in the films limiting the heat transfer only to the upper facet of the films resulting in limited cooling capabilities. In the case of a microstructured CNT film, i.e., fin structure, the grooves in the film enable better coolant flow and heat dissipation from the fins towards the surrounding medium via convective fluxes. Further optimization of the geometry/location of the fin structures for a given specific system can operate with different fin heights, lateral dimensions, and fin densities resulting in even more efficient cooling in critical areas.

Computational fluid dynamics and thermoelectric finite element models were developed to study the steady-state laminar coolant flow (with Reynolds number of ~ 1800 at the nozzle exit for 0.5 l/min flow rate) and also the temperature distribution for both the finned CNT and bare reference chips. The obtained velocity values of the modeled flow fields were used to approximate empirically the corresponding average heat transfer coefficients h at different locations of the experimental geometry, which were subsequently used in the heat-flow calculations. Depending on the local flow rates, the typical values for h varied from 20 up to 500 $\text{W m}^{-2} \text{K}^{-1}$, that are in good agreement with the values published for impingement gas flow conditions.¹⁷ Because of the relatively low temperatures and small surface areas of the hot spots, the losses caused by the heat radiation are neglected in the thermal model, i.e., the heat transport is restricted to conductive and convective fluxes. The heat-flow model, in which we use flow dependent film coefficients and



FIG. 3. (Color online) Graph in the left panel shows chip temperatures measured for chip-on-substrate (red plots) and for the corresponding CNT 10×10 fin array-on-chip-on-substrate assemblies (blue plots) under various heating powers and N_2 flow rates. The graph in the right panel shows the results of a comparative experiment in which a finned copper cooler (10×10 array) was used.

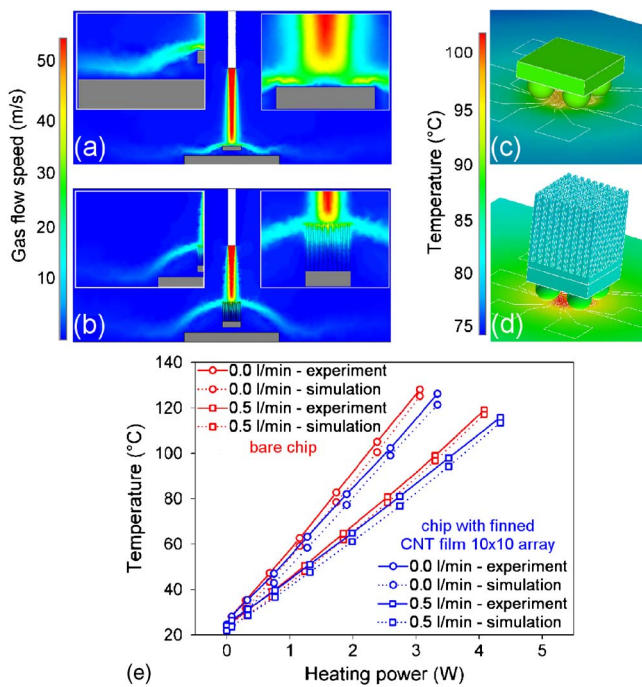


FIG. 4. (Color online) Steady-state solutions for coolant flow velocity and temperature distribution for a chip without and with a finned cooler. Panels (a) and (b) show plots for the coolant velocity; insets show more detailed plots of the areas nearby the surfaces. Panels (c) and (d) show plots of the temperatures at 3 W heating power and 0.5 l/min coolant flow. The fins are considered as a bulk medium with an effective density of 350 kg m^{-3} , and with an effective anisotropic thermal conductivity of $300/30/30 \text{ W m}^{-1} \text{ K}^{-1}$. Specific heat of $650 \text{ J kg}^{-1} \text{ K}^{-1}$ is used. The graph in panel (e) compares the experimental and computational results for the power vs temperature curves for both natural convection and forced convection (0.5 l/min) conditions.

temperature dependent material parameters, gives good account on the chip temperatures we measured for various experimental conditions (Fig. 4).

In summary, a simple and efficient cooling method is demonstrated for chip thermal management using laser-patterned CNT fins transferred and mounted on the back side of the chips. This method provides a light-weight, mechanically stiff, effective, and facile alternative of large, much heavier metal block coolers or fluid based complex systems. Our technique employs conventional manufacturing methods and thus provides an easy protocol to transfer and integrate nanotube arrays onto the presently used silicon platforms. Since the resulting cooling efficiency—in terms of power density—is in the range of microcircuit needs ($\sim 100 \text{ W cm}^{-2}$), the carbon nanotube coolers could serve as efficient parts of these devices. Tailoring nanotube structure to obtain higher thermal conductivity,¹⁷ improvement and optimization of the chip-nanotube thermal interface,¹⁸ en-

larging the interface surface via using double-sided vertical arrangements, optimizing fin-array geometry (spacing, width, and height of fins, heat sink base dimension) (Ref. 19) as well as location, nanotube length, and forest density, and improved gas flow efficiency could lead to additional enhancement of the power dissipation reported here.

The authors acknowledge the financial support received from the Academy of Finland (Project No. 209414), the Nokia Scholarship, and the Focus Center New York for Electronic Interconnects.

- ¹A. Bar-Cohen and W. M. Rohsenow, *ASME J. Heat Transfer* **106**, 116 (1984).
- ²R. E. Simons, V. W. Antonetti, W. Nakayama, and S. Oktay, *Heat Transfer in Electronic Packages in Microelectronics Packaging Handbook* (Chapman and Hall, New York, 1997), Vol. 1, Chap. 4, p. 314.
- ³D. Tuckerman and R. Pease, *IEEE Electron Device Lett.* **2**, 126 (1981).
- ⁴Y. Peles, A. Kosar, C. Mishra, C.-J. Kuo, and B. Schneider, *Int. J. Heat Mass Transfer* **48**, 3615 (2005).
- ⁵M. S. Dresselhaus and P. C. Eklund, *Adv. Phys.* **49**, 705 (2000).
- ⁶M. J. Biercuk, M. C. Llaguno, M. Radosavljevic, J. K. Hyun, A. T. Johnson, and J. E. Fischer, *Appl. Phys. Lett.* **80**, 2767 (2002).
- ⁷Y. Wu, C. H. Liu, H. Huang, and S. S. Fan, *Appl. Phys. Lett.* **87**, 213108 (2005).
- ⁸J. Hone, M. C. Llaguno, M. J. Biercuk, A. T. Johnson, B. Batlogg, Z. Benes, and J. E. Fischer, *Appl. Phys. A: Mater. Sci. Process.* **74**, 339 (2002).
- ⁹M. Zhimin, R. Morjan, J. Anderson, E. E. B. Campbell, and J. Liu, *Proceedings of the IEEE 55th Electronic Components and Technology Conference*, Lake Buena Vista, FL, 31 May 2005, pp. 51–54.
- ¹⁰M. Zhimin, J. Anderson, and J. Liu, *Proceedings of the IEEE 6th High Density Microsystem Design and Packaging and Component Failure Analysis Conference*, Shanghai, China, 30 June 2004, pp. 373–376.
- ¹¹A. Y. Cao, V. Veedu, X. S. Li, Z. Yao, M. N. Ghasemi-Nejhad, and P. M. Ajayan, *Nat. Mater.* **4**, 540 (2005).
- ¹²X. S. Li, A. Y. Cao, Y. J. Yung, R. Vajtai, and P. M. Ajayan, *Nano Lett.* **5**, 1997 (2005).
- ¹³S. Talapatra, S. Kar, S. K. Pal, R. Vajtai, L. Ci, P. Victor, M. M. Shaijumon, S. Kaur, O. Nalamasu, and P. M. Ajayan, *Nature Nanotechnology* **1**, 112 (2006).
- ¹⁴See EPAPS Document No.E-APPLAB-90-021711 for the consecutive steps of device fabrication; soldering the flip chip onto the substrate; usage of solder flux; and finally a block of aligned nanotube structure along its Cr/Cu sputtered side was positioned and soldered on the chip by a fine-placer. This document can be reached via a direct link in the online article's HTML reference section or via the EPAPS homepage (<http://www.aip.org/pubservs/epap.html>).
- ¹⁵A. Y. Cao, P. L. Dickrell, W. G. Sawyer, M. N. Ghasemi-Nejhad, and P. M. Ajayan, *Science* **310**, 1307 (2005).
- ¹⁶L. A. Brignoni and S. V. Garimella, *IEEE Trans. Compon., Packag. Manuf. Technol., Part A* **22**, 399 (1999).
- ¹⁷P. Kim, L. Shi, A. Majumdar, and P. McEuen, *Phys. Rev. Lett.* **87**, 215502 (2001).
- ¹⁸S. T. Huxtable, D. G. Cahill, S. Shenogin, L. R. Osisik, P. Barone, M. Usrey, M. S. Strano, G. Siddons, M. Shim, and P. Keblinski, *Nat. Mater.* **2**, 731 (2003).
- ¹⁹J. G. Maveety and H. H. Jung, *IEEE Trans. Compon. Packag. Technol.* **25**, 459 (2002).