Coulomb blockade and single-electron devices

One interesting limit of nanoelectronics are devices with impedances strongly influenced by the positions of single electrons.

Imagine a transistor where the source-drain current is controlled by the presence or absence of a single electron on a controlling gate.

The plan:
• Coulomb blockade physics intro
• Single junctions
• Single-island, double-junction systems
• Single-island, double-junction + a gate: the single-electron transistor.
• Many islands and junctions: the electron turnstile

Coulomb blockade physics

As we’ve mentioned before, for any classical conductors coupled together electrostatically, it’s possible to define a capacitance that relates the charge on each conductor to the potential between the conductors:

\[ Q_i = \sum_j C_{ij} V_j \quad \Rightarrow \quad E = \frac{1}{2} \sum_i \sum_j \frac{Q_i Q_j}{C_{ij}} \]

Two conductors with a mutual capacitance \( C \) attached to opposite terminals of a battery with voltage \( V \) build up a charge \( Q = CV \) (one +, one -).

Work done in charging the capacitor: \( Q^2/2C \).

That charge does is a polarization charge and does not have to be quantized in units of \( e \)…
Coulomb blockade physics

Capacitances: (assume embedding dielectric $\kappa$)

$$C = 4\pi \kappa \epsilon_0 d \left( 1 + \alpha + \frac{\alpha^2}{1 - \alpha^2} + \ldots \right), \quad \alpha = \frac{a}{2l}$$

Can make systems where charging energy is larger than $k_B T$.

Room temperature $\rightarrow C \sim 3 \times 10^{-18} \text{ F}$. For vacuum, $\rightarrow a \sim 28 \text{ nm}$.

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Coulomb blockade physics

*Coulomb blockade* occurs when charging energy for moving a single electron through a system (e.g. $\sim e^2/2C$) exceeds the available (thermal) energy.

Ideally no current flows at $T = 0$ in a fully blockaded circuit.

A blockaded circuit element has a definite number $n$ electrons in its blockaded configuration.

Blockade may be lifted / broken if:

- A sufficiently large bias is applied, so that $eV$ exceeds the charging energy.
- An additional capacitively coupled electrode is used to offset the charging energy.
Coulomb blockade: a single tunnel junction

Ideal version: charge accumulates and voltage across capacitor ramps up at rate given by $I/C$ until $eV$ exceeds charging energy $e^2/2C$.

At that point it is possible for one electron hops across the tunnel barrier, and the voltage drops back down….

$$\Delta E = \frac{(Q \pm q)^2}{2C} - \frac{Q^2}{2C} = \frac{e^2}{2C} \left(1 \pm \frac{Q}{e/2}\right)$$

Result: voltage across current-biased single junction is expected to oscillate as shown, with a typical frequency $f = I/e$.

In practice, this effect is nearly impossible to see: there is always stray capacitance in the leads that dwarfs the junction capacitance. The current source charges up the stray capacitance, and then the system acts like….
Coulomb blockade: a single tunnel junction - voltage bias

Voltage-biased junction.

Here no current flows unless $V$ exceeds the charging threshold, $V_c = e/2C$. This is Coulomb Blockade.

Actual capacitor charge not quantized, b/c it’s a polarization charge (can vary continuously by slightly shifting all electrons in leads).

Shown here is typical $IV$ curve for voltage biased single junction (blue). High temperature limit = red; zero temperature ideal case = green.

Single-island, double-junction

One of the most commonly examined cases is that of an island connected to a voltage supply by two junctions:

What happens to the current through this system as the voltage $V_a$ is varied?
The Coulomb staircase

We know:

\[ Q_1 = C_1 V_1 \]
\[ Q_2 = C_2 V_2 \]
\[ V_a = V_1 + V_2 \]

For \( n \) electrons on the island,

\[ Q = Q_2 - Q_1 = -ne \]

If the total capacitance of the island is \( C_{eq} = C_1 + C_2 \),

\[ V_1 = \frac{1}{C_{eq}} (C_2 V_a + ne) \]
\[ V_2 = \frac{1}{C_{eq}} (C_1 V_a - ne) \]

Total electrostatic energy:

\[ E_s = \frac{Q_1^2}{2C_1} + \frac{Q_2^2}{2C_2} = \frac{1}{2C_{eq}} (C_1 C_2 V_a^2 + Q^2) \]

When an electron hops off the island, the voltage source must transfer that charge as well as any polarization charge required to keep the total voltage drop equal to \( V_a \).

Suppose an electron tunnels through \( 2 \) off the island, so that \( Q' = Q + e \), and \( n' = n - 1 \).

The voltage across \( 1 \) becomes \( V_1' = V_1 - e/C_{eq} \), so a polarization charge must flow through the voltage source to compensate.

Total work done to pass \( n_2 \) charges through junction 2:

\[ W_{2}(n_2) = -n_2 e V_a \frac{C_1}{C_{eq}} \]

Total work done to pass \( n_1 \) charges through junction 1:

\[ W_{1}(n_1) = -n_1 e V_a \frac{C_2}{C_{eq}} \]
The Coulomb staircase

Total energy of whole circuit after moving \( n_1 \) electrons through junction 1 and \( n_2 \) through junction 2:
\[
E(n_1, n_2) = E_s - W_s = \frac{1}{2C_{eq}} (C_1 C_2 V_s^2 + Q^2) + \frac{eV}{C_{eq}} (C_n + C_s n_s)
\]

Now, at \( T = 0 \), only tunneling changes that lower this energy are allowed. Tunneling a particle through 2 changes the energy by:
\[
\Delta E_2^\pm = \frac{(Q \pm e)^2}{2C_{eq}} \pm \frac{Q^2}{2C_{eq}} \pm \frac{eV C_1}{C_{eq}} \pm \frac{e}{C_{eq}} \left( \pm (en - V_a C_1) \right)
\]
Upper sign = tunneling electron off island

Similarly, tunneling a particle through 1 changes the energy by:
\[
\Delta E_1^\pm = \frac{e}{C_{eq}} \left[ \pm \frac{e}{2} (en + V_a C_2) \right]
\]

The Coulomb staircase

Start with a neutral island \( (n = 0) \). Combining the two expressions,
\[
\Delta E_{1,2}^\pm = \frac{e^2}{2C_{eq}} \pm \frac{eV C_{2,1}}{C_{eq}}
\]
For \( C_1 = C_2 = C \), the energy change is positive (forbidden) unless
\[
|V_a| > \frac{e}{C_{eq}} = \frac{e}{2C}
\]

This is Coulomb blockade.

Suppose one electron has already tunnelled onto the island. Then the (Fermi) energy of the island is raised by \( e^2/C_{eq} \), and no charge can flow until \( V_a \) crosses a new threshold, \( 3e/C_{eq} \).
The Coulomb staircase

The result is the Coulomb staircase:

Only resolvable when there’s a strong asymmetry in resistances, such as \( R_1 >> R_2 \). Then, as soon as an electron tunnels out of junction 1, one from 2 comes in to maintain \( n \).

Voltage drop across 1 for equal capacitance case:

\[
V_1 = \frac{V_a + ne}{2C_{eq}}
\]

Size of current step:

\[
\Delta I = \frac{\Delta V_1}{R_1} = \frac{e}{2CR_1}
\]

Requirement on resistances to see these effects:

\[
\Delta E \Delta t > h \quad \rightarrow \quad \left( \frac{e^2}{C_{eq}} \right) \left( RC_{eq} \right) > h \rightarrow R >> \frac{h}{e^2}
\]

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The single-electron transistor: single-island, double-junction + gate

Can redo the same kind of electrostatic and stability analysis, but now include gate:

\[
Q_g = C_g(V_g - V_2)
\]

\[
Q = Q_2 - Q_1 - Q_g = -ne + Q_p
\]

\[
C_{eq} = C_1 + C_2 + C_g
\]

\[
V_1 = \frac{1}{C_{eq}} \left( (C_g + C_2)V_a - C_gV_g + ne - Q_p \right)
\]

\[
V_2 = \frac{1}{C_{eq}} \left( C_1V_a + C_gV_g - ne + Q_p \right)
\]
The single-electron transistor

\[ E_s = \frac{1}{2C_{eq}} (C_g C_1 (V_a - V_g)^2 + C_g C_2 V_g^2 + C_1 C_2 V_a^2 + Q^2) \]

\[ W_s(n_1) = -n_i \left[ eV_g \frac{C_2}{C_{eq}} + e(V_a - V_g) \frac{C_g}{C_{eq}} \right] \]

\[ W_s(n_2) = -n_i \left[ eV_a \frac{C_1}{C_{eq}} + eV_g \frac{C_g}{C_{eq}} \right] \]

\[ \Delta E_1^g = \frac{(Q \mp e)^2}{2C_{eq}} \pm \frac{e}{C_{eq}} [(C_g + C_2)V_a - C_g V_g] \]

\[ = \frac{e}{C_{eq}} \left[ \frac{e}{2} (en - Q_p) + (C_g + C_2)V_a - C_g V_g \right] \]

\[ Q_p \] accounts for “offset charge” on or near island.

\[ \Delta E_2^g = \frac{(Q \pm e)^2}{2C_{eq}} \pm \frac{e}{C_{eq}} \left[ C_1 V_a + C_g V_g \right] \]

\[ = \frac{e}{C_{eq}} \left[ \frac{e}{2} (en - Q_p - C_1 V_a - C_g V_g) \right] \]

Gate allows one to effectively vary the charge on the island!

The single-electron transistor

Again, at \( T = 0 \), only transitions that \textit{lower} the total energy are allowed.

Define a new voltage: \( V_g' = V_g + Q_p / C_g \)

Forward tunneling then requires:

\[ \mp \left[ en + (C_g + C_2)V_a - C_g V_g \right] > \frac{e}{2} \]

Backward tunneling requires:

\[ \pm \left[ en - C_1 V_a - C_g V_g \right] > \frac{e}{2} \]

Gate voltage can be used to tune system in and out of Coulomb blockade!

- At the right gate voltages, the coupling to the gate can offset the energy cost that would otherwise exist for hopping an electron on or off the island.
- The gate voltage required to change the conductance is offset from its “ideal” value if there is excess charge coupled to the island \( (Q_p) \).
The single-electron transistor

Gate voltage can be used to tune system in and out of Coulomb blockade!

Diagram for $C_g = C = C_1 = 2C$.

Shaded regions: no conduction; definite number of charges on island.

Points of intersection: system can lower its energy by changing number of charges on island; conductance peak.

Plots like this from experimental data are called “diamond plots”.

Notice that modulating gate charge by less than one electron can change from blockaded to conducting conditions.

Single-electron transistor

For fixed $V_a$, source-drain conductance is periodic in $V_g$ with peaks spaced by $e/C_g$.

Red lines = high conductance near zero source-drain bias.

Magnitude of conductance when not in blockade regime:

$$G_{\text{max}} = \frac{1}{R_1 + R_2}$$
Single-electron transistor - finite $T$

Blockade gets smeared out at finite temperature.

In case of SET, Coulomb blockade peaks (conductance as a function of gate voltage) take on a width in gate voltage (since $k_B T$ can make up for extra energy required):

$$\frac{G}{G_{\text{max}}} = \cosh^{-2}\left(\frac{e(C_e/C_m) \cdot (V_g - V_g^0)}{2.5k_B T}\right)$$

Curve calculated for $k_B T = 0.05 \frac{e^2}{C_{eq}}$

The R-SET and other variations

We’ve been discussing C-SETs - gate charge capacitively influences island charge.

It’s also possible to build R-SETs, in which the gate is actually connected (!) to the island via a large ($\gg R_1, R_2$) resistor.

For that case, island charge can truly be changed by the gate.

It’s also possible, if done carefully, to substitute large resistances for the tunnel junctions. This is called a resistive SET - see Krupenin et al., JAP 90, 2411 (2001):
The single-electron turnstile

More complicated structures can give rich behavior. One can make a turnstile device that ideally lets through only one electron at a time. This particular approach dissipates significant power.

The single-electron pump

This version is quasi-adiabatic: By cycling $U_1$ and $U_2$ out of phase with each other, once can pump electrons through the two islands with minimal power dissipation. Dominant errors in these approaches due to cotunneling. Can be minimized by increasing number of tunnel junctions....
Summary:

- Classical electrostatics plus slow charge relaxation (tunneling?) plus (low temperatures or small sizes) can lead to Coulomb blockade devices.
- Single junction can show CB effects if arranged carefully.
- Double junction can exhibit Coulomb staircase.
- Additional gates allow single-electron transistors, switchable from low (ideally zero) to high conductance by moving a single electronic charge on or off the gate.
- More complicated arrangements permit pumping of electrons, ideally one at a time.

Next time:

Implementations of single-electron devices

Single-electron logic: voltage logic

Single-electron logic: charge logic

Problems with industrial implementation
Single-electronics: the story so far

- For small enough structures and low enough temperatures, Coulomb charging effects can determine the conducting properties of circuits.
- Two-terminal double-junction devices can show complicated (Coulomb staircase) $IV$ curves.
- Multiterminal devices can show transistor-like functionality, with substantial current switching modulated by the positions of individual electrons.

Main driver for possible applications:
- Need $E_c = e^2/C_{eq} \gg k_BT$, so want smallest junctions possible.

Sizes of things: for $E_c = 50 \ k_BT$ at 300 K, need $C_{eq} \sim 0.1 \ aF$.

Implementations of single electron devices

Several different ways of making SETs:
- Shadow-evaporation + oxidation of Al
  Most common approach, best suited for large-scale fabrication of arrays.
- Oxidation of silicon
  Compatibility / ease of integration with Si
- Chemically-aided approaches
  Trapped nanoparticles; AFM contacting; molecular devices.
Shadow evaporation and oxidation of Al

Takes advantage of ease of growth of thin, high-quality \( \text{Al}_2\text{O}_3 \) for tunnel barriers.

Uses geometry to make smallest possible junctions.

- Double-layer resist for e-beam lithography leads to overhang.
- Evaporate at an angle. Then oxidize for controlled length of time.
- Evaporate straight down - forms first junction. Then oxidize for controlled length of time.
- Third evaporation forms second junction.

Lateral size of junction overlap determined by resist thicknesses (well-controlled) and angles (also well-controlled).

By tilting in different directions, can make complicated structures:
Shadow evaporation and oxidation of Al

2d Josephson junction array
image from Mooij, Delft, Netherlands

Inverter from two coupled SETs
image from Mooij, Delft, Netherlands

SET on tip of drawn glass fiber
image from Bell Labs

Local oxidation
images from Matsumoto et al., APL 68 34 (1996).

- Recall tunneling transistor: local electrochemical oxidation (anodization) used to convert continuous Ti strip into island + insulating tunnel barriers.
- Painstaking fabrication, but payoff is SET with some room-temperature functionality.
Even for an island as small as this, getting room temperature oscillations is a real challenge.
Nanocrystalline silicon

Tan et al. work with doped nanocrystalline Si deposited by PECVD.

Nanocrystalline regions surrounded by amorphous matrix.

Oxidize for known amount of time to form barriers.

Gated laterally.

Grain size is sufficiently small that some gate modulation of conductance is detectable even at 300 K.

Still a far cry from a workable device.
Trapped nanoparticles

One approach: use chemical fabrication to make nanoparticles for use as SET islands.
Trap particles between lithographically created electrodes.
Electrostatic trapping in above – nanoparticle drawn to region of high local electric field as source/drain are biased.

Trapped nanoparticles

Alternative:
• Start with continuous metal electrodes on top of insulated metallic substrate, to be used as a gate.
• Dust surface to decorate with nanoparticles, such as chemically synthesized CdSe nanocrystals.
• Break into separate source-drain electrodes by “electromigration”, and sometimes nanocrystal ends up ideally positioned to act as island.
Nanoparticles on surfaces

- Can decorate surface with tethered nanoparticles, in this case Au colloid.
- Insulating layer = self-assembled monolayer of thiol-terminated alkane chains.
- Scanned probe microscope tip as drain electrode: Coulomb staircase.


Nanoparticles on surfaces

Special tip can incorporate gate, too, for SET action.

images from Gurevich et al., APL 76, 384 (2000).
Clear technological challenges:

- Reliable fabrication of sub-10 nm structures with little or no variation for room temperature Coulomb blockade physics.
- Tuning of “environmental characteristics” such as stray capacitance.
- Reliable (self-controlling?) tunnel junctions.
- Control of single electronic offset charges: individual charged defects can have effects identical to random offset voltages on gates!

Incentives:

- Dense integration.
- Possible ultralow power operation (reversible?).
- Ultimate limits of switching technology.

Technology possibilities

Voltage-based logic:

- Very similar to typical CMOS logic: high voltage = logic high; low voltage = logic low.
- Nonmonotonic drain current as function of gate voltage opens up designs not possible with regular MOSFET devices.

Charge-based logic:

- Since SETs can sense presence/absence of single electronic charges, use positions of charges to represent data / logic values.
- Some novel architectures possible, since charge positions can cause alter voltages capacitively, which can then move charges: e.g. Quantum Cellular Automata.
Voltage-based logic:

It is possible, with SETs, to achieve voltage gain. That is, the output voltage modulation of a circuit can be greater than the input voltage modulation:

\[ K_V = \left| \frac{\partial V_{\text{out}}}{\partial V_G} \right| \]

Circuit designers can treat SET-based logic gates like conventional logic gates (keeping current designs) and leave the details up to the hardware folks.

Good point: SET characteristics (oscillatory response to \( V_G \)) mean that one SET can sometimes replace more than one regular MOSFET.

CMOS inverter: 2 transistors of opposite types

SET inverter: 1 SET + resistive load.
### Voltage-based logic:

**Problems:**
- Analysis shows that, for acceptable device performance, either temperatures must be very low, or devices must be extremely small. ..
  \[ k_B T \sim 0.01 \frac{e^2}{2C} \]
  
  This can be mitigated slightly (factor of 3) by using arrays of tunnel junctions, but at cost of lower packing density and more challenging fabrication.
- “Off”-state leakage leads to power consumption problems comparable to highly-scaled CMOS.

### Charge-based logic:

- Try to use positions of individual charges to represent “1”s and “0”s.
- Have switching action depend on charge state of device (necessary for logic).

**Potential advantage:** does not require substantial current flow for operation. Power consumption could therefore be advantageous.

**Tricky problem:** single charge errors now become very important.
Charge-based logic:

One approach analyzed in detail = SET “parametron”.

Has series of islands with “middle” islands asymmetrically coupled.

Clock signal pushes electrons along chain.

Summary of problems:

- Temperature range of operation places great restrictions on device sizes.
  - Such small devices are likely to suffer tremendous variability.
  - Further, (especially in semiconductor devices) quantum level spacing effects (which superpose on the charging energies and alter the heights of the blockade conductance peaks) are likely to be significant.

- Background charges are also a serious problem.
  - Some chance that this may be self-correcting at sufficiently tiny scales, but not at all clear.

- Characteristic resistances (~ 10 kΩ) mean that for realistic capacitances these devices are unlikely to operate at high speeds.
Prognosis:

Single electron devices are unlikely to be the technology that replaces CMOS at the few nm scale, unless there is a major breakthrough in fabrication, performance, or architectures. SEDs more likely to find applications in niche areas:

- Nonvolatile memory
- Electrometry
- Metrology standards

Next time:

- Applications of single electron devices
- Capacitance standard
- Electrometers - the scanning SET
- Thermometry
- Intro to the rf-SET