Advanced Microprocessor Architecture

Instructor

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Office hours: By prior arrangement

Course Information

Class: T/Th 10:50am-12:05pm DH 1075
Web: http://www.owlnet.rice.edu/~elec525/
Labby: TBA

Course Description

The class will explore the current trends and future directions of processor microarchitecture, looking ahead to billion transistor chips. The focus of the class will be on high-performance processor and memory architectures. We will explore various techniques designed to maximize parallelism and improve performance. We will also look at the influence of technology on processor and memory architectures and how that may affect future processor designs. Knowledge of the material covered in COMP/ELEC 425 will be assumed. The class will include in-depth coverage of topics such as:

• Front end design (e.g. branch prediction, instruction fetch, trace caching)
• Exploiting instruction-level parallelism (e.g. VLIW, simultaneous multithreading, processor coupling)
• Memory system issues (e.g. caching, prefetching, bandwidth)
• Technology implications (e.g. scaling, power)
• Future processor architectures (e.g. MAJC, Raw, reliability)

The class will include a mix of lectures and discussions on assigned readings of recent publications. Students will be responsible for leading and participating in these discussions. A course project that can be performed in groups will also be required.

Prerequisites

COMP/ELEC 425 or equivalent and programming experience

Readings

Selected papers from the literature to be provided on the course web page
Discussions

Most classes will consist of a discussion of two papers on a particular topic in microprocessor architecture. All students are expected to read the papers. In addition, for each discussion, a student will be assigned to prepare a presentation of the papers and come prepared with a set of important questions to kick off a discussion of the topic.

Project

The project will involve investigating some aspect of high-performance microprocessor architecture via simulation. For example, you may develop and evaluate new memory operations, storage architectures, or core organizations. I suggest that the project investigate one of the areas that we will be discussing during class, but you are free to propose any research topic in microprocessor architecture. You may work on these projects in groups.

Grading

20% Discussion Leading
20% Discussion Participation
60% Project

Students with Disabilities

Any student with a documented disability needing academic adjustments or accommodations is requested to speak with me during the first two weeks of class. All discussions will remain confidential. Students with disabilities will need to also contact Disability Support Services in the Ley Student Center.