

DETOL Verification

**Multiprocessing Pipelined Matched Filter
Architecture Using Online Arithmetic.**

ELEC 423

April 23, 2003

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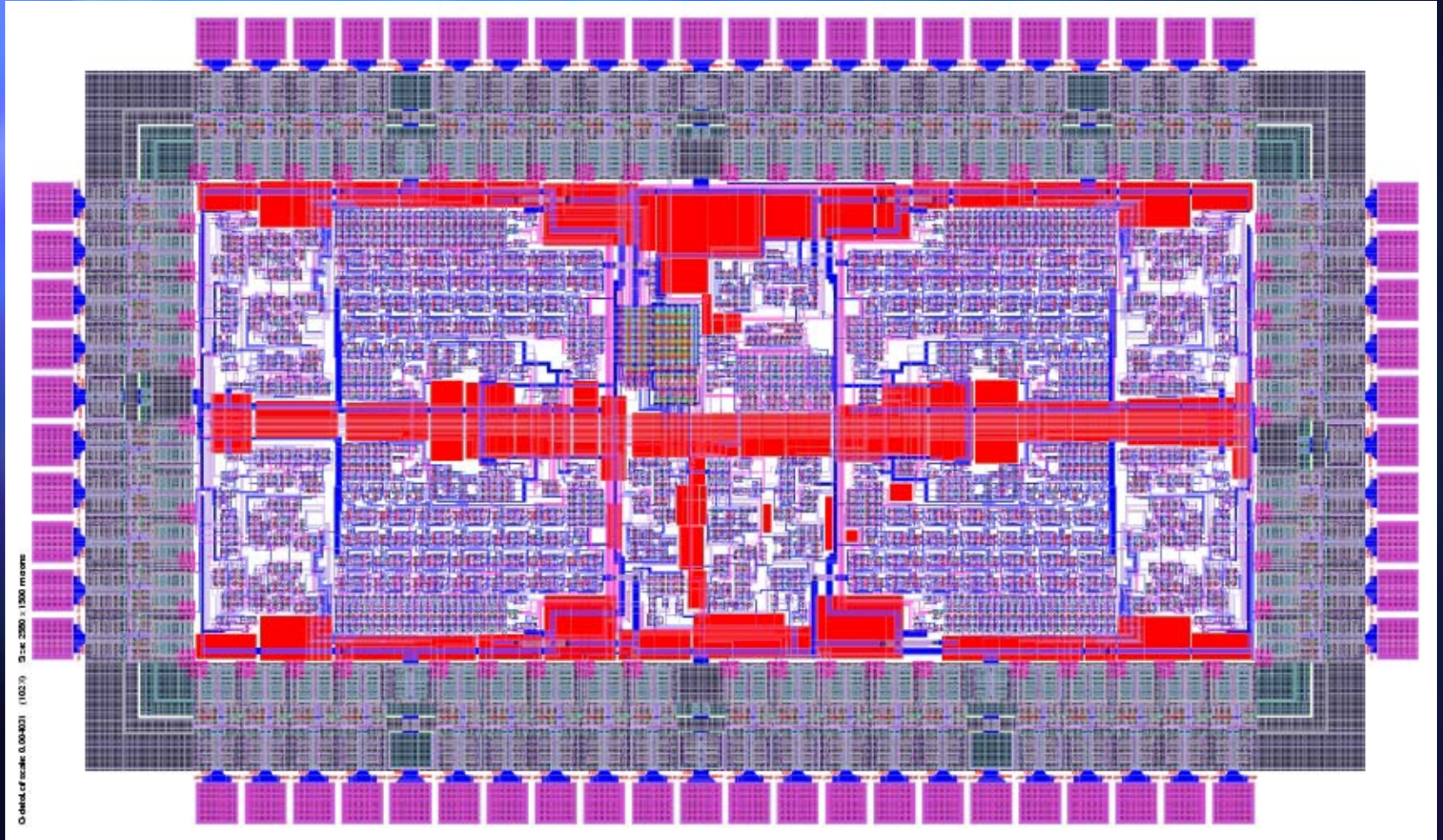
Predrag Radosavljevic

Nils Bagge

Outline

- Review of Functional Description
- Functional Test Results
- Speed Test Results
- Yield

Chip

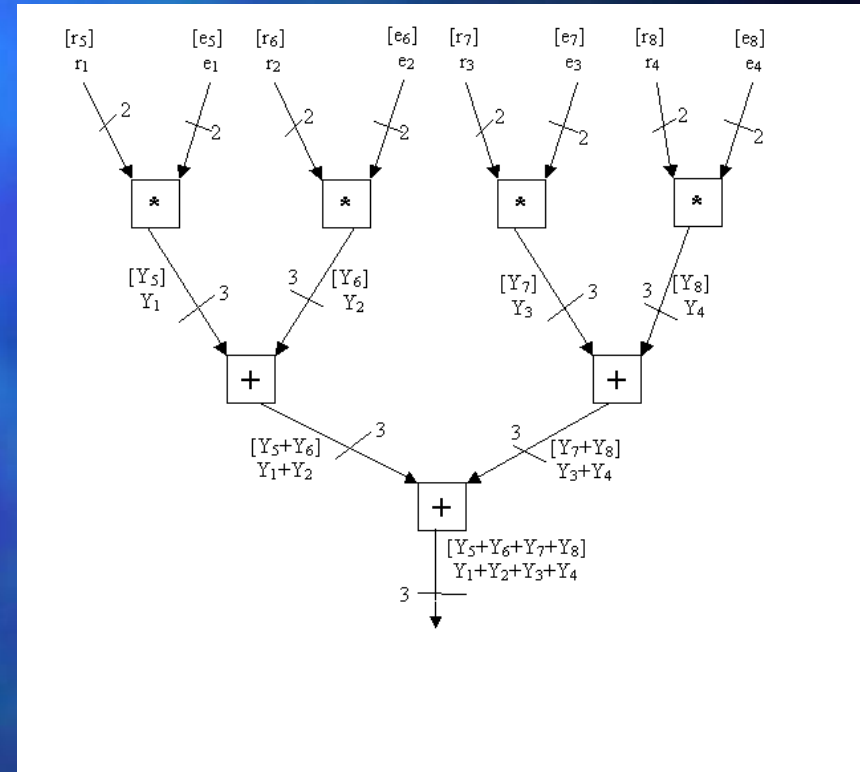


Functional Description: Pin Map

	StBit0	StBit1	StBit2	StBit3	Vdd	StBit4	Restart	Precision	Clock A	Clock B	GND	Out3	Out2	Out1	N/C	Ready	Accum	Mode	Vdd	N/C	N/C	N/C
In[1]y[2]	<h1>DETOL</h1>																				N/C	
In[1]y[1]																					In[3]y[2]	
In[1]x[2]																					In[3]y[1]	
In[1]x[1]																					In[3]x[2]	
GND																					In[3]x[1]	
In[2]x[1]																					GND	
In[2]x[2]																					In[4]x[1]	
In[2]y[1]																					In[4]x[2]	
In[2]y[2]																					In[4]y[1]	
N/C																					In[4]y[2]	
N/C																					N/C	
N/C																					N/C	
Add1[2]																					N/C	
Vdd	N/C																					
Add1[3]	Vdd																					
Add1[1]	N/C																					
Mul1[3]	N/C																					
Mul1[2]	N/C																					
Mul1[1]	Vdd																					
GND	N/C																					
Add2[2]	N/C																					
Add2[3]	N/C																					
Add2[1]	N/C																					
N/C	N/C																					
N/C	N/C																					
Vdd	N/C																					
N/C	N/C																					
N/C	N/C																					
N/C	N/C																					
N/C	N/C																					

Functional Description

- Multiprocessing
Pipelined Matched
Filter architecture
using online
arithmetic



Functional Tests Performed

- Tests performed using TLA & Omnilab:
 - Full-precision (4-digit online output, 12-bit)
 - Fast Precision-1 (1-digit online output)
 - Full-matched filter mode
 - Online addition only (mult. bypassed)
- Goals:
 - Verify online multiplier functionality
 - Verify online adder functionality
 - Verify overall matched filter functionality

Functional Test Results

- Successes:

- Online multiplier works properly
 - Very complex → Very gratifying!
- Online adder works as designed
- Proper transitions of the PLA states
- Final Output:
 - Correct for Fast Precision-1

- Flaw:

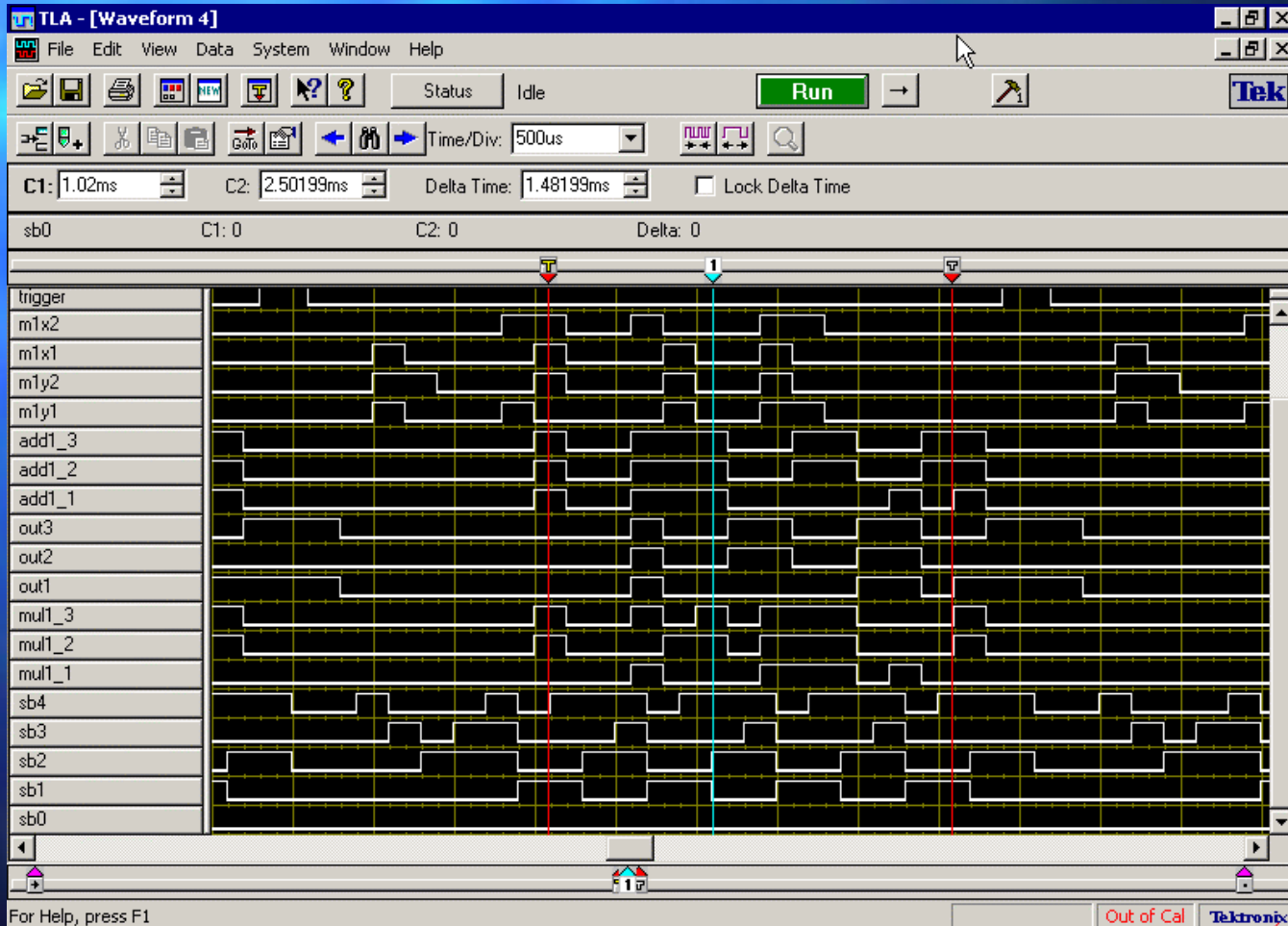
- Final Output incorrect for Full Precision
- Suspected error: final adder receiving out-of-sync control signals (PLA load/clear of pipeline/adder registers)

Speed Test Results

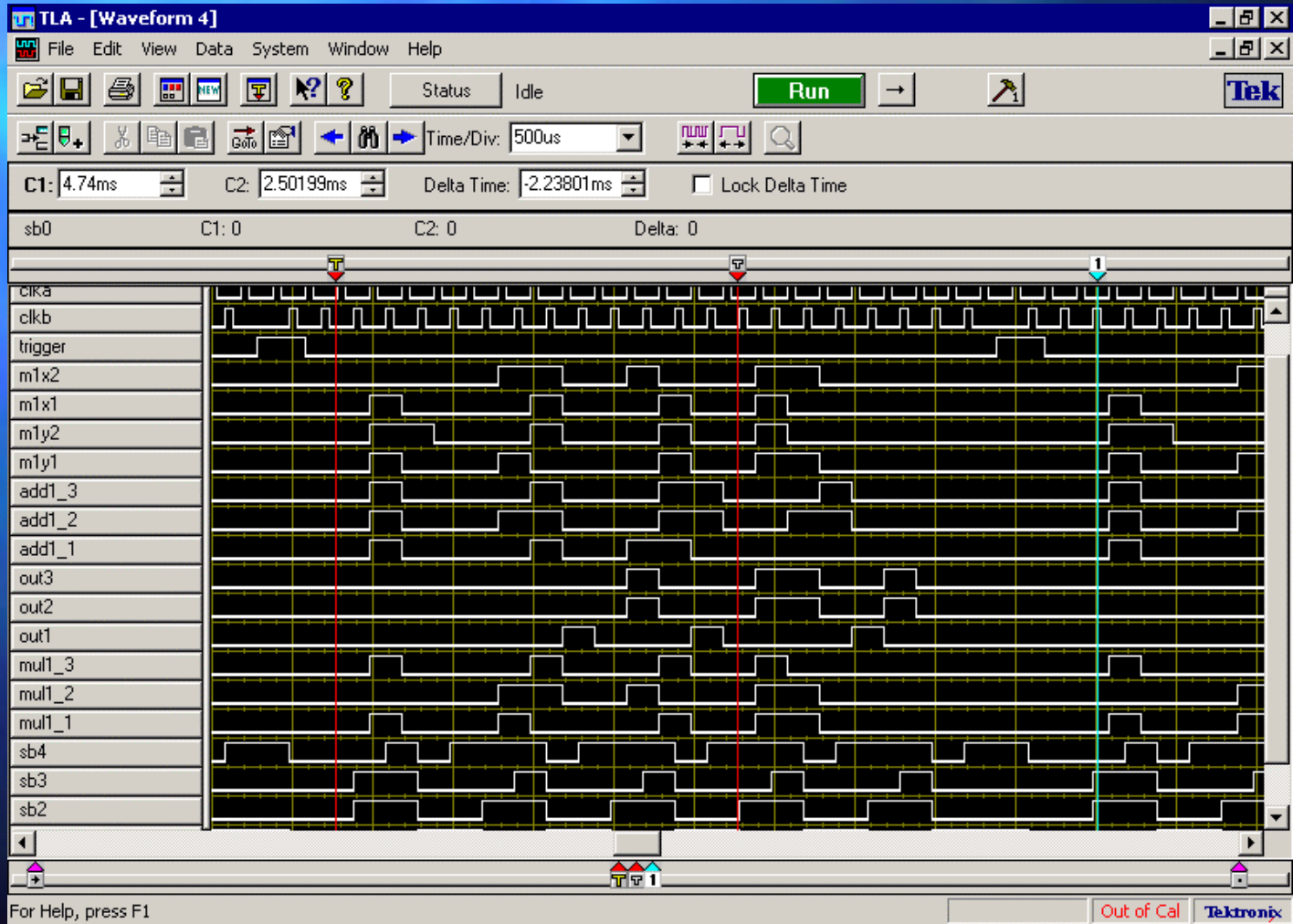
- Highest usable clock frequency:
 - ~ 45 MHz $\Leftrightarrow \sim 22$ ns clock period.
 - Glitching becomes excessive at 50MHz.
 - Roughly same as Spice analysis suggested:
42.18MHz

Testing Portfolio

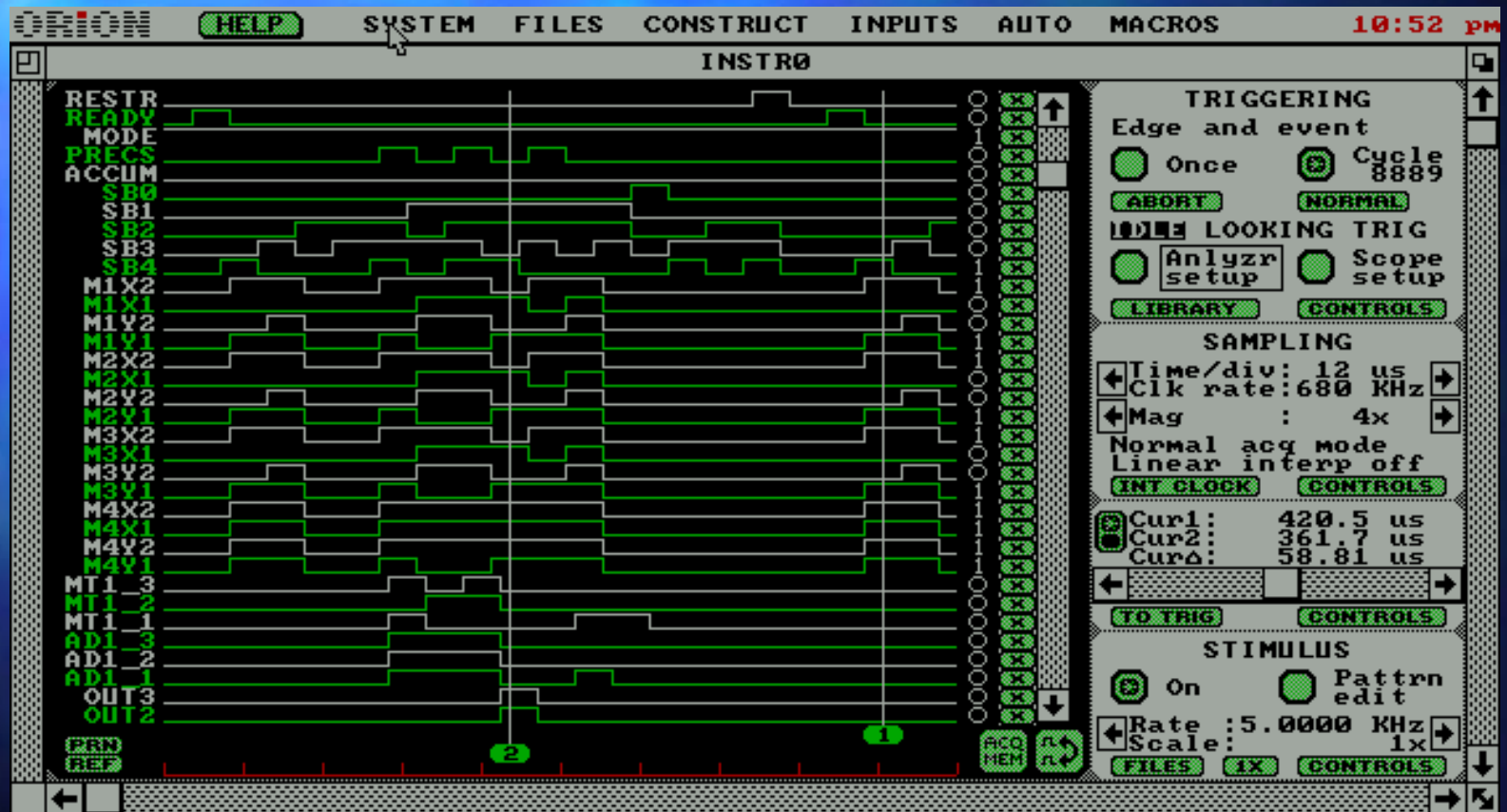
Testing Portfolio: Mode-1 Full-Precision



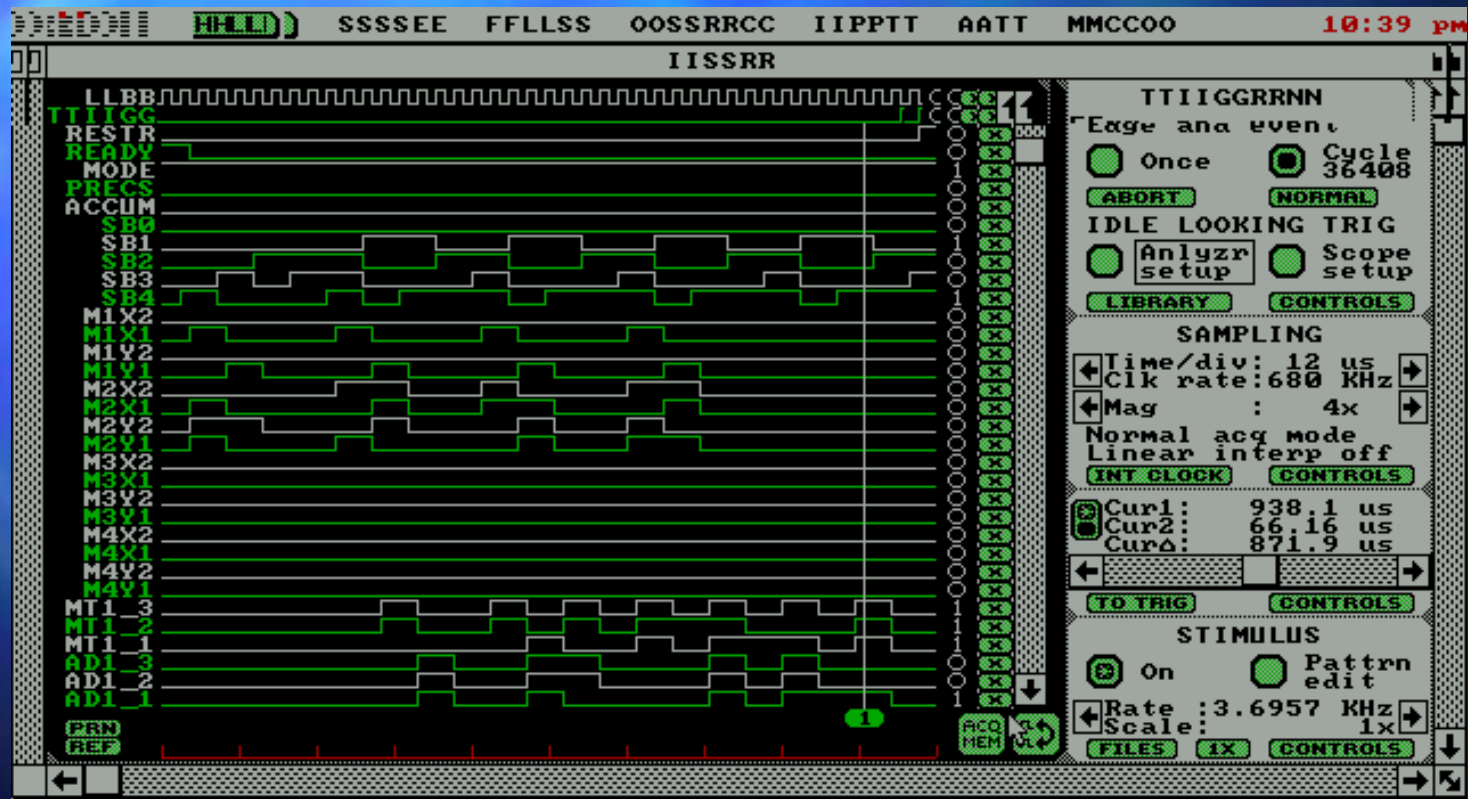
Testing Portfolio: Mode-0 Full-Precision



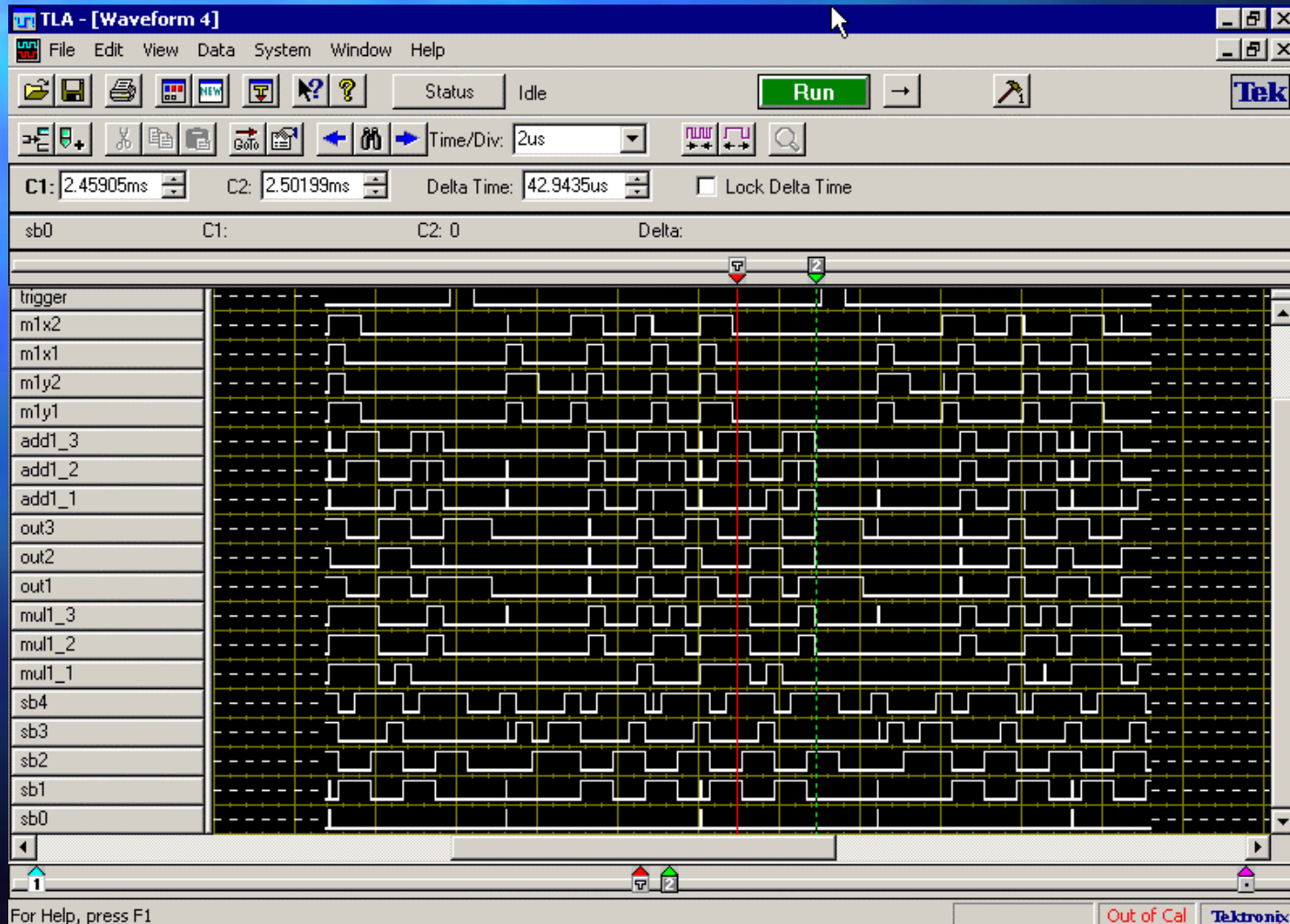
Testing Portfolio: Mode-1 Precision-1



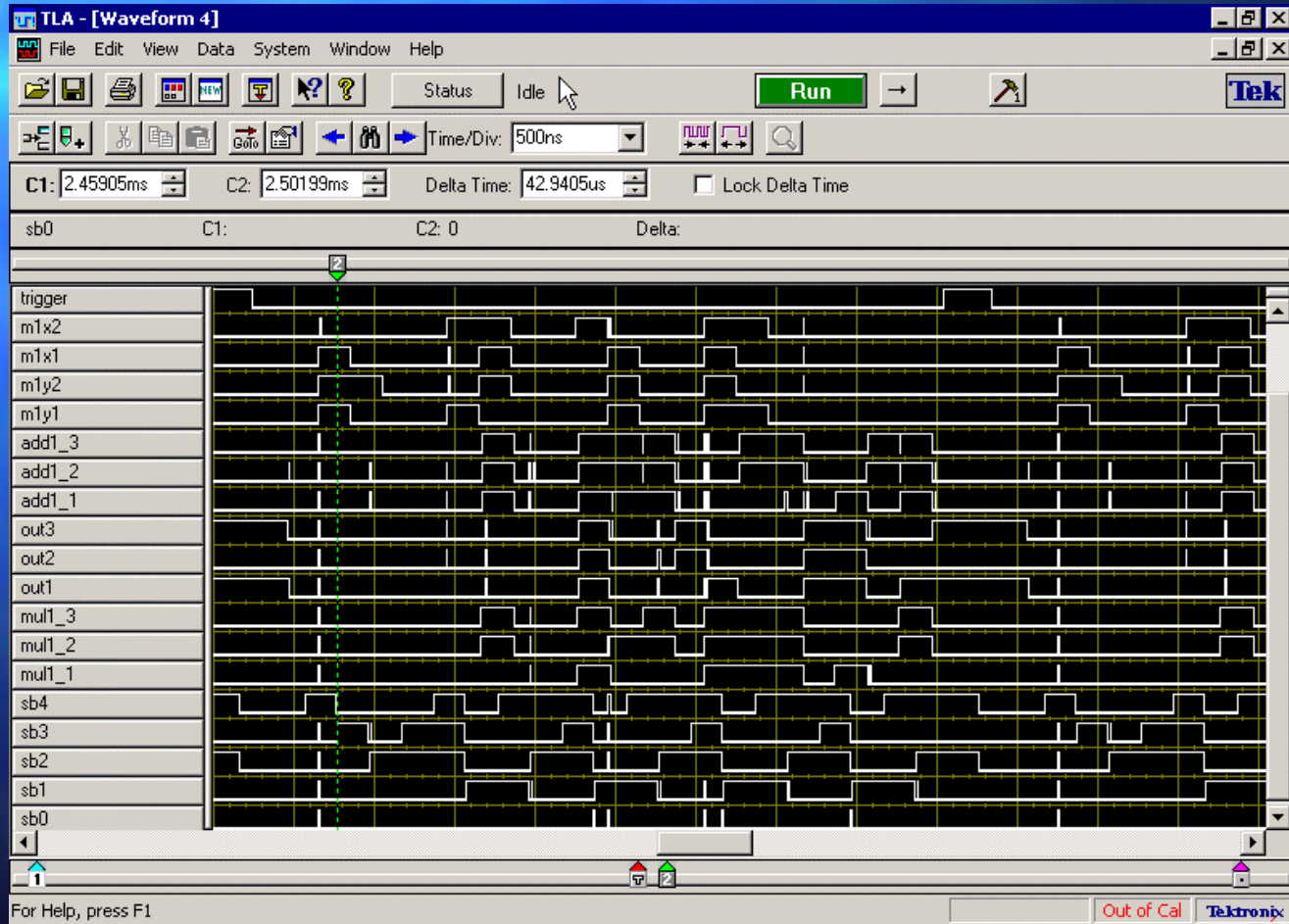
Testing Portfolio: Mode-1 Full-Precision



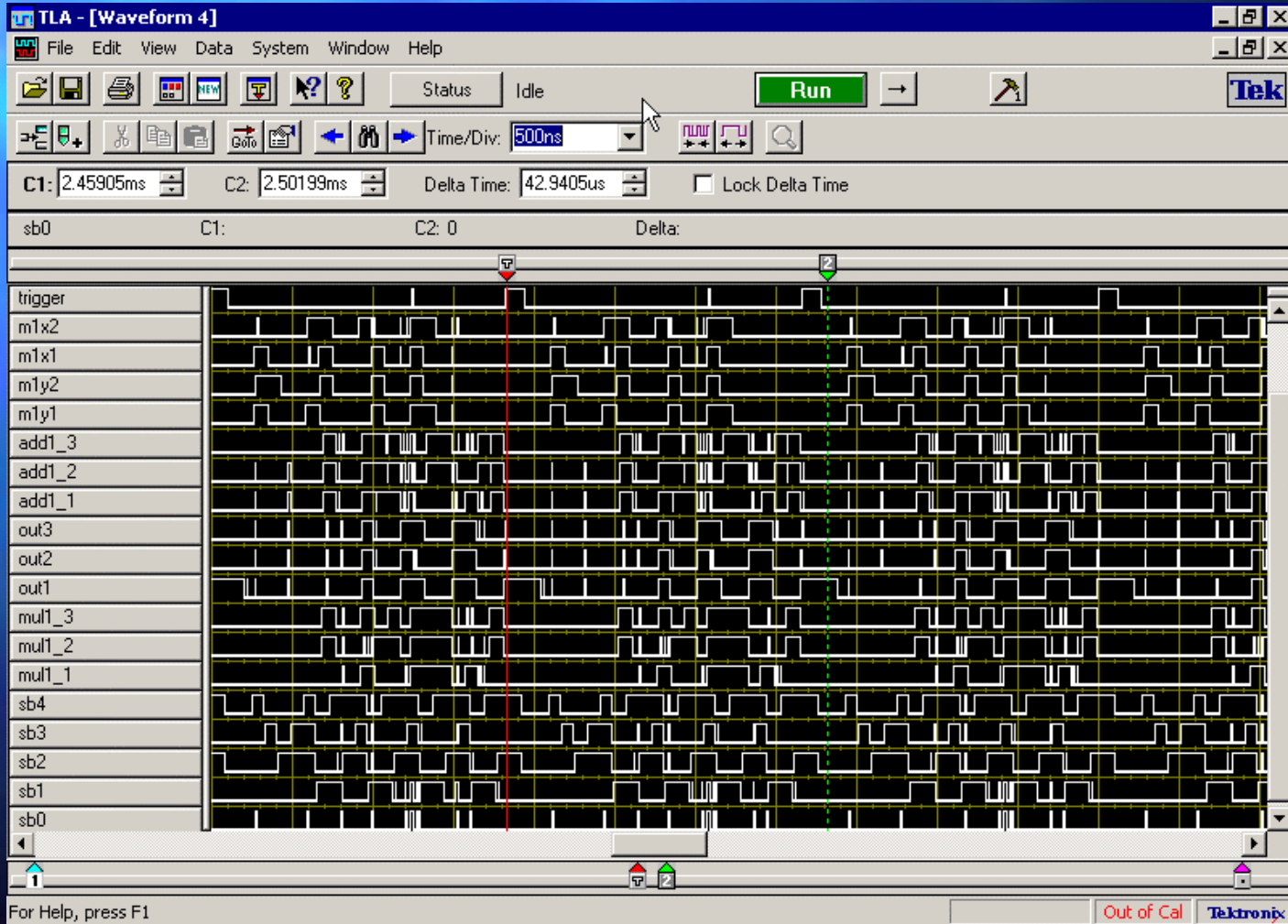
Testing Portfolio: Speed Test (f=10MHz)



Testing Portfolio: Speed Test (f=20MHz)



Testing Portfolio: Speed Test (f=50MHz)



Conclusions

- Work-around: Matched-filtering *still* possible using two multipliers on chip (thanks to redundancy in design)
- Using multi-chip configuration, can still achieve higher data-rate/longer spreading codes
- Yield: all 5 chips are working identically

Conclusions

SPREADING CODE LENGTH 8

FULL OPERATION MODE



FULL OPERATION MODE

SPREADING CODE LENGTH 32 (HARD DETECTION)

