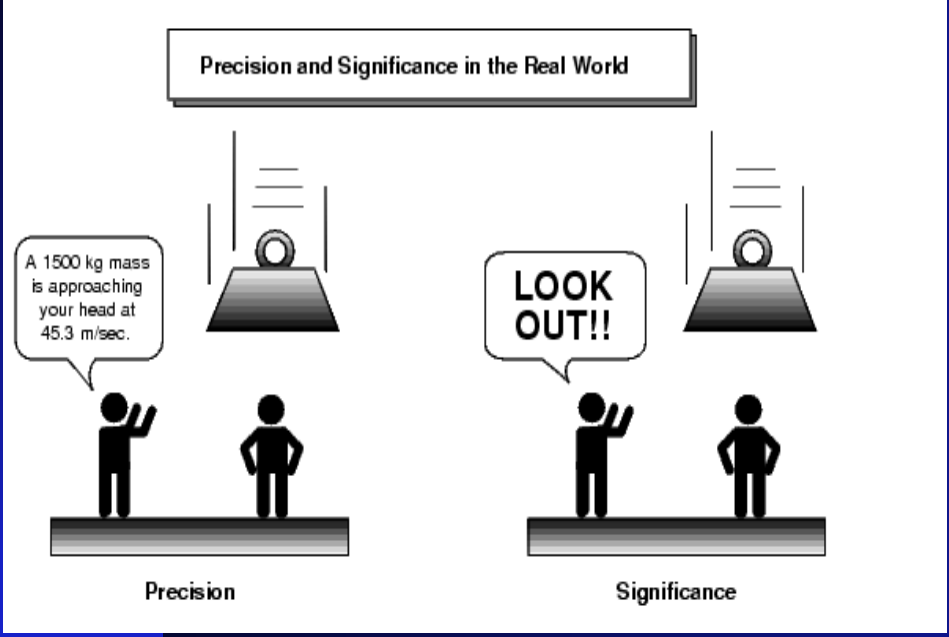
Testing Arbiter:
FUZZY LOGIC CONTROLLER



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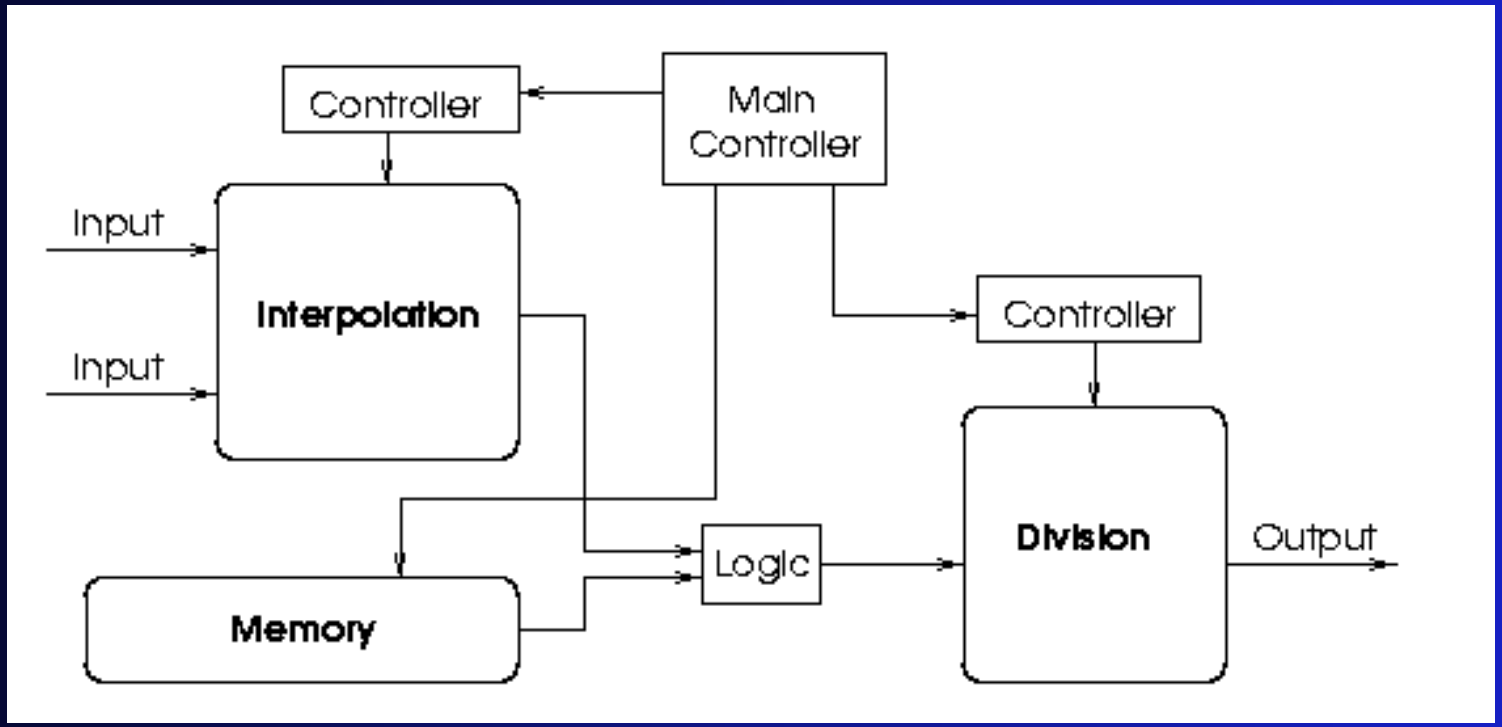
Functional Description

- Purpose: To Approximate Human Reasoning
- Basic Block Diagram:



Importance of Design-For-Test

- Computationally Intensive
  - Loads 9 functions, 2 inputs -> Outputs 1 answer
- Observability & Controllability are VERY IMPORTANT!
  - Although we already had 15,000 transistors on 40 pin pad, we made it a point to include extensive testing structures

Testing Structure

- 4 to 16 Decoder
  - Controls transmission gates that inputs to bus
  - Watch 8 internal signals at a time
- Observe a total of 120 internal signals!
- Signals observed include:
  - PLA state bits, intermediate answers, loaded register values

Initial Full Chip Test

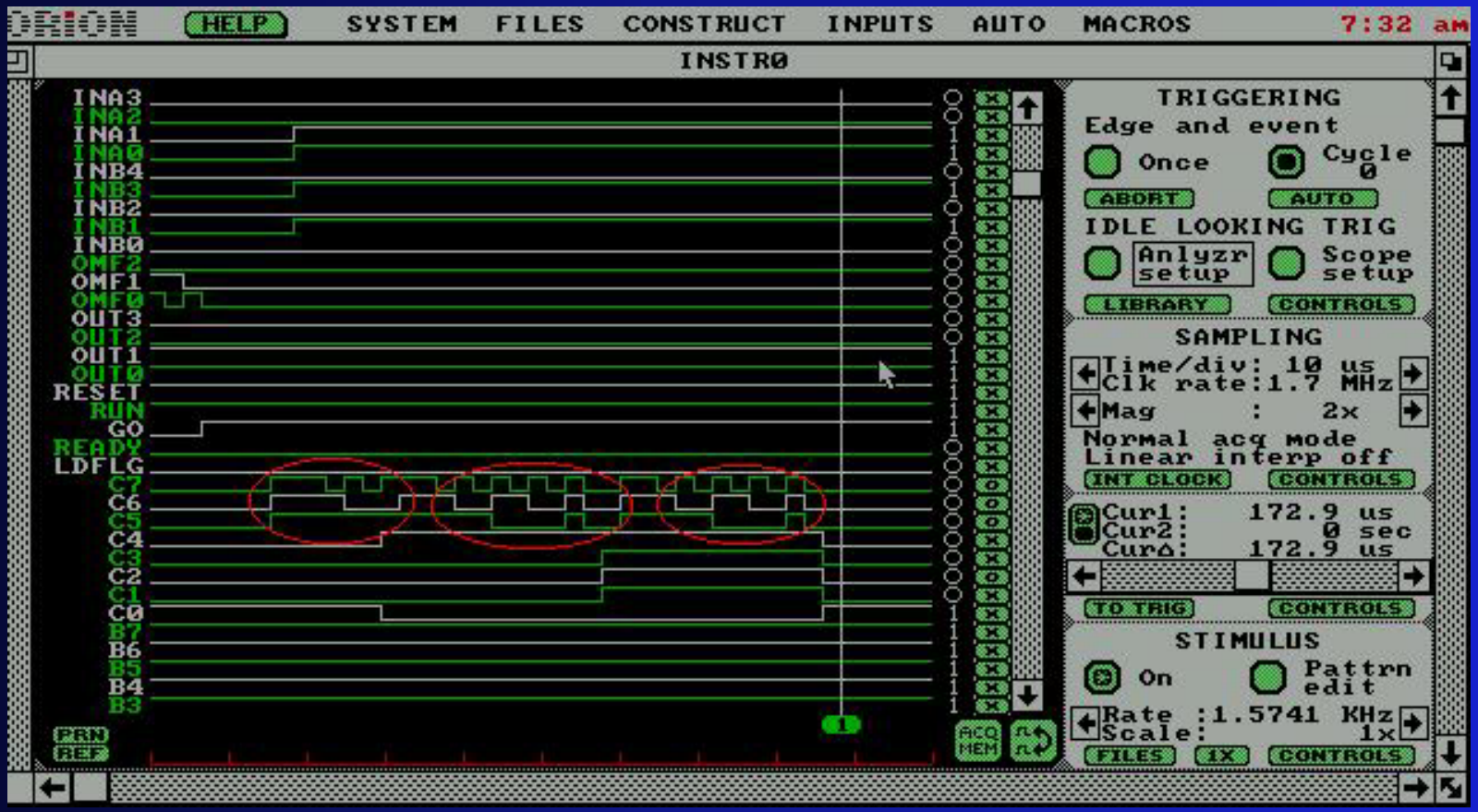
- Used 3 full-length test vectors
- IT WORKS!!!
  - Kinda…
  - Answer consistently off by 1

Testing Strategy

- 1) Test PLA:
  - Observed state transitions of each PLA
  - All 5 PLA's are correct!
- 2) Test major components:
  - Interpolation
  - Division
  - Memory

Unit Test 1: INTERPOLATION

- Interpolation values converge to prediction

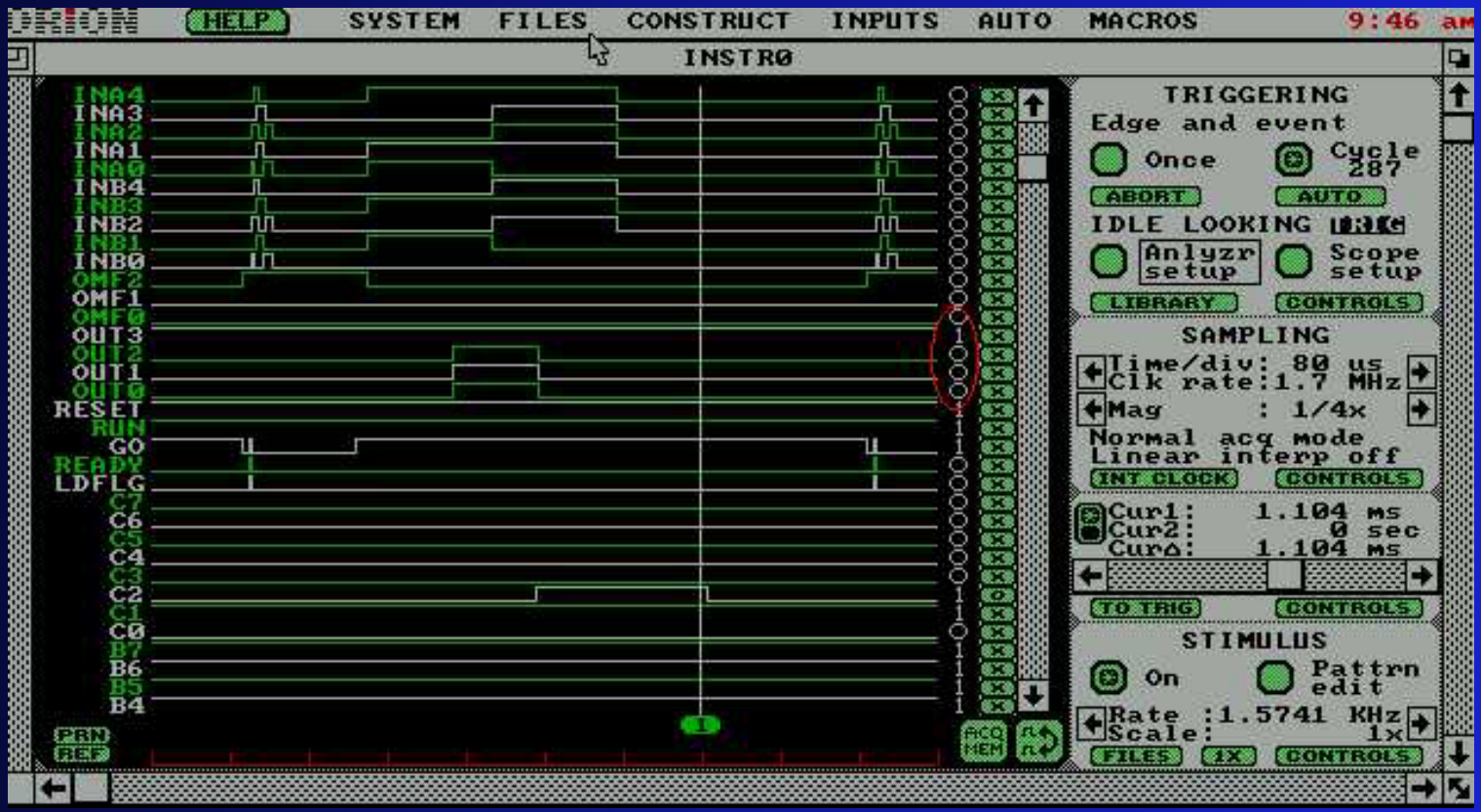


Unit Test 2: DIVISION

- 11 bit non-restoring division
- Final stage of chip
  - Need to verify final stage works by itself, *independent* of upstream pipeline's correctness.
  - Controllability needed.

Division: Controllability

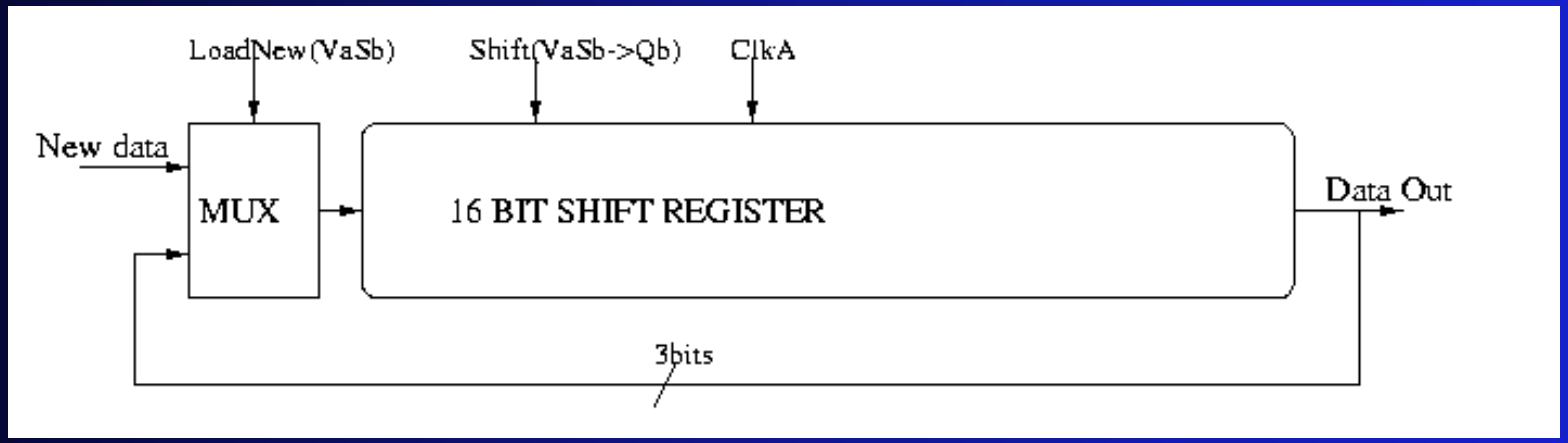
- Control inputs to division so output is predictable irrespective of upstream pipeline's results



Unit Test 3: Memory

- Hypothesis:
  - It makes sense that complex structures like division are correct, or else the answer will be messed-up. If the answer is only off by 1, maybe loading memory is off

- 16 bit Ring Shift-Register

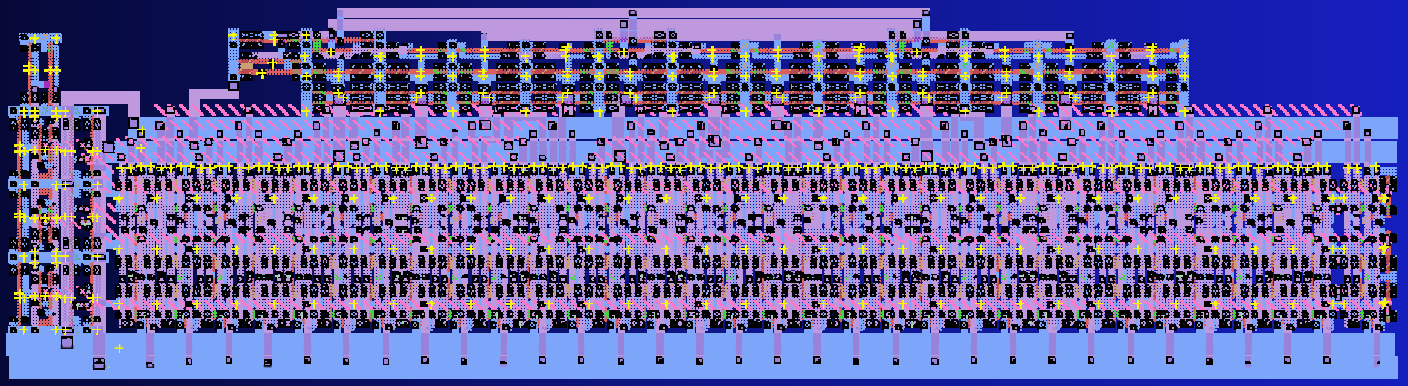


Problem Discovered!!

- Shift-register corrupts a few values
- Test sequence example:
  - Input: 0 0 1 2 3 4 5 6 7 7 4 5 2 1 0 0
  - Observed: 0 0 1 2 3 4 5 6 7 **4** 4 5 2 **0** 0 0
- At two points, register loads in a neighboring value

Possible Reasons

- Back-flow between registers
  - Prevented by inverters between latches
- Strength of latch content signals differ
  - Logic 0 corrupts adjacent logic 1
- Control signal skew
  - May cause extra shift in certain registers



Final Analysis

- Speed: 27 MHz. Predicted: 63 MHz.
- Yield: 100%
  - Recognizing error is constant across chips
- Error is small and easy to fix.

In Conclusion…

- We have:
  - Demonstrated that a programmable fuzzy logic architecture is possible on small chip-size.
  - Experienced first-hand the importance of Design-for-Test
- Special thanks to:
  - Dr. Cavallaro
  - AMD
  - MOSIS