Final Project for ELEC422

FastCPU

Arshad Hussain

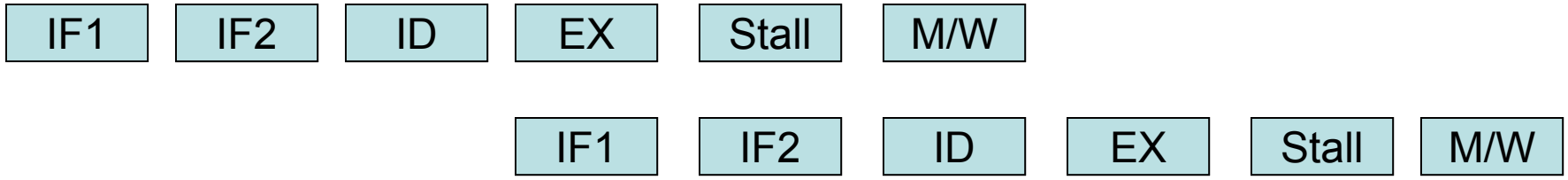
Lixin Su

Jun Tang

What is FastCPU?

- 6 stage pipeline RISC processor
- 16 bit instructions set
- 16 bit internal data bus
- 8 bit I/O bus
- 8-bit CLA adder, 8bit bi-dir Barrel Shifter, 4 bit Multiplier
- Tap Controller for serial scan of PC out on a pin for debugging.
- Total number of transistors 8500 (without Pad Frame)
- Fastest clock speed: 42 MHz
- Status:
  - Design and testing of all blocks are complete
  - IRSim testing from pads is complete!
  - Mission accomplished!

Our Pipeline

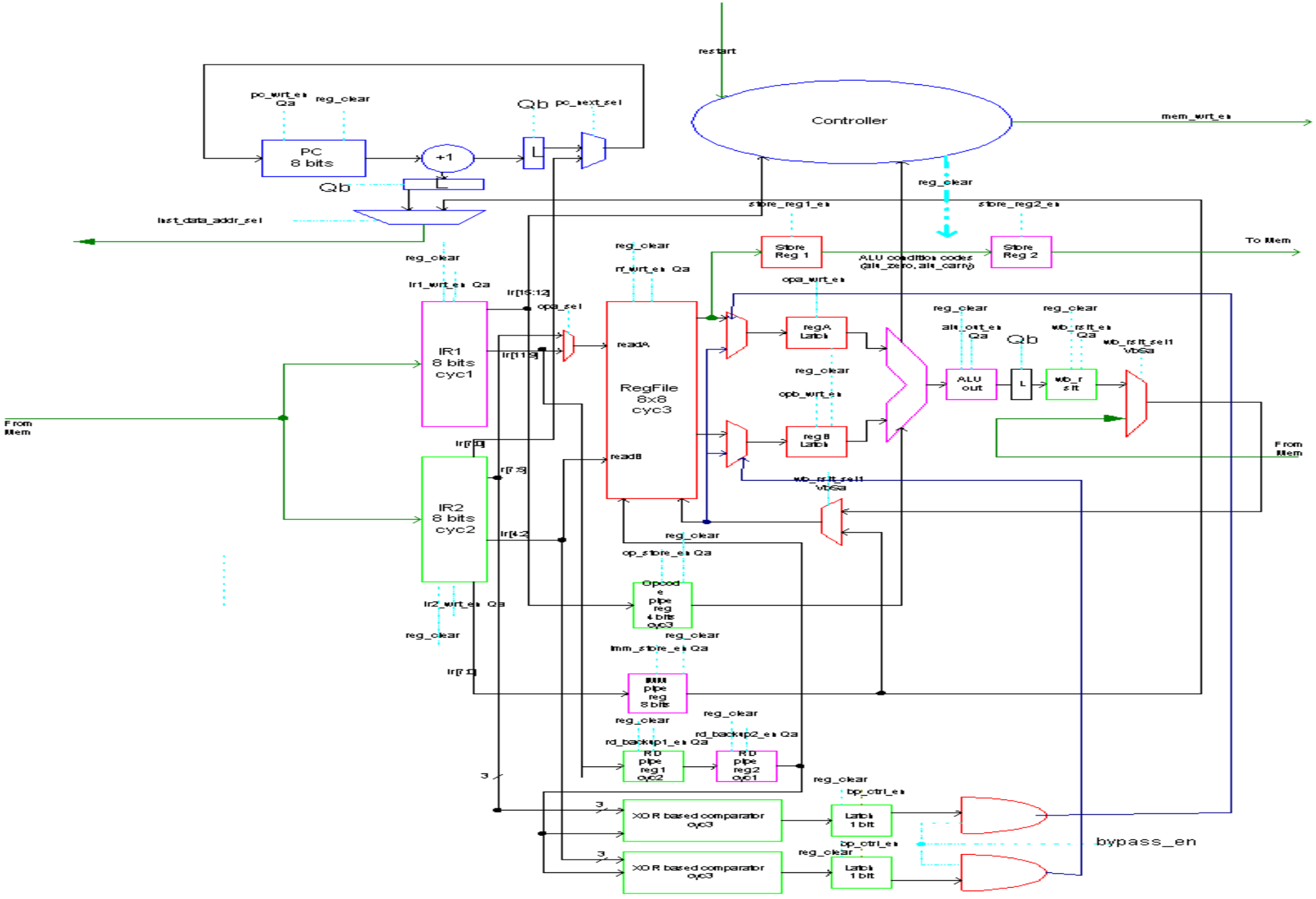


1. Stall is inserted to avoid the structural hazard (Due to the pin number limitation, the data and instruction memory accesses share the same 8 pins).
2. There must be an ALU operation before conditional branches. The target address of the next instruction can always be resolved in the ID stage of the current instruction.
3. Data forwarding is used in the ID stage when needed.

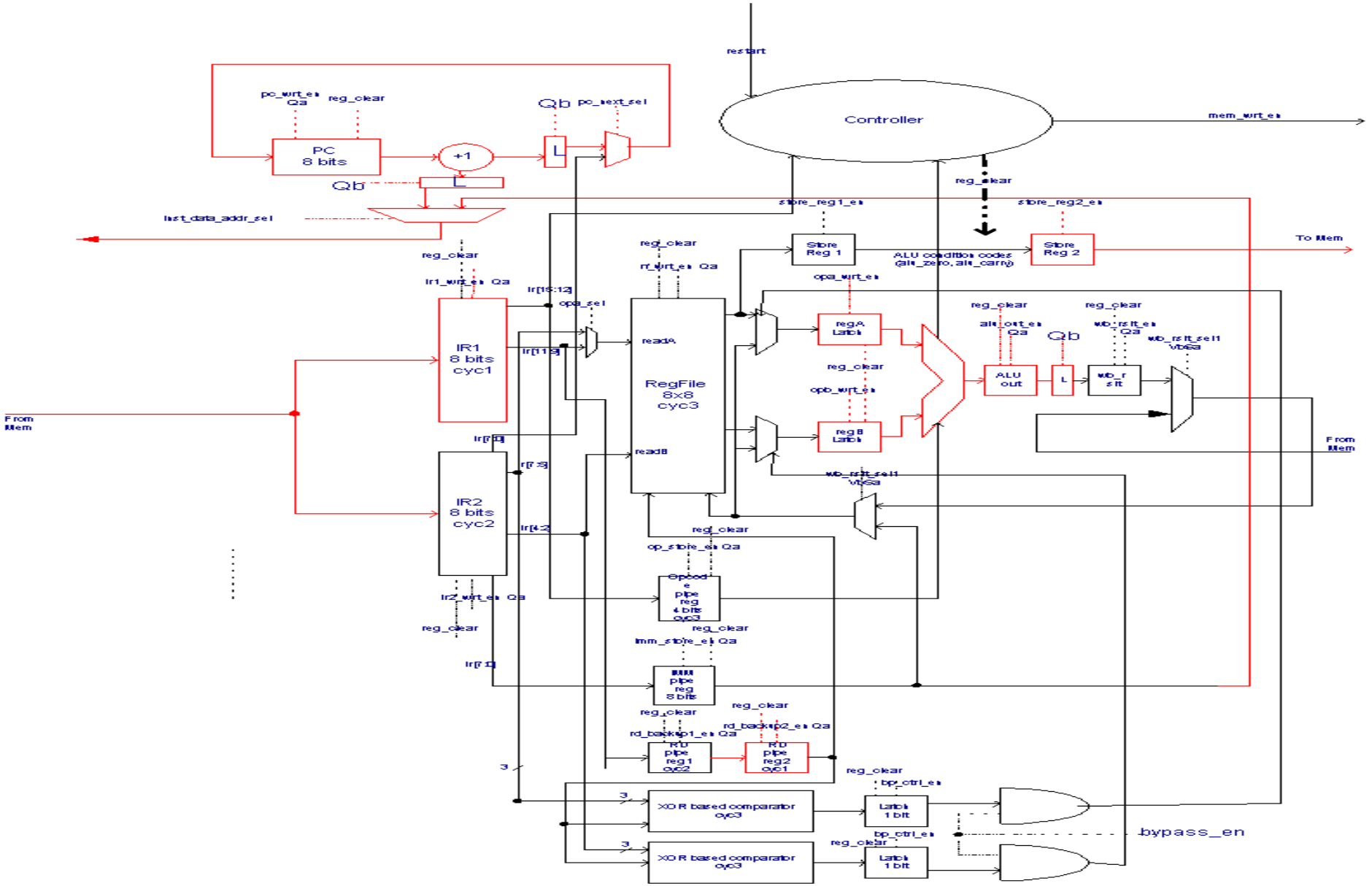
Instruction Set

operation	op code (15-12)	destination register (11-9)	source register (7-5)	target register (4-2)
ADD	1000	Rd	Rs	Rt
SUB	1001	Rd	Rs	Rt
MULT	1010	Rd	Rs	Rt
AND	1011	Rd	Rs	Rt
OR	1100	Rd	Rs	Rt
NOT	1101	Rd	Rs	N/A
SLL	0101	Rd	Rs	Rt
SRL	1111	Rd	Rs	Rt
JR	0000	N/A	Imm Addr	
JC	0001	N/A	Imm Addr	
JZ	0011	N/A	Imm Addr	
LW	0100	Rd	Imm Addr	
SW	0010	Rs	Imm Addr	
LWI	0101	Rd	Imm Data	
NOP	0110			
END	0111			

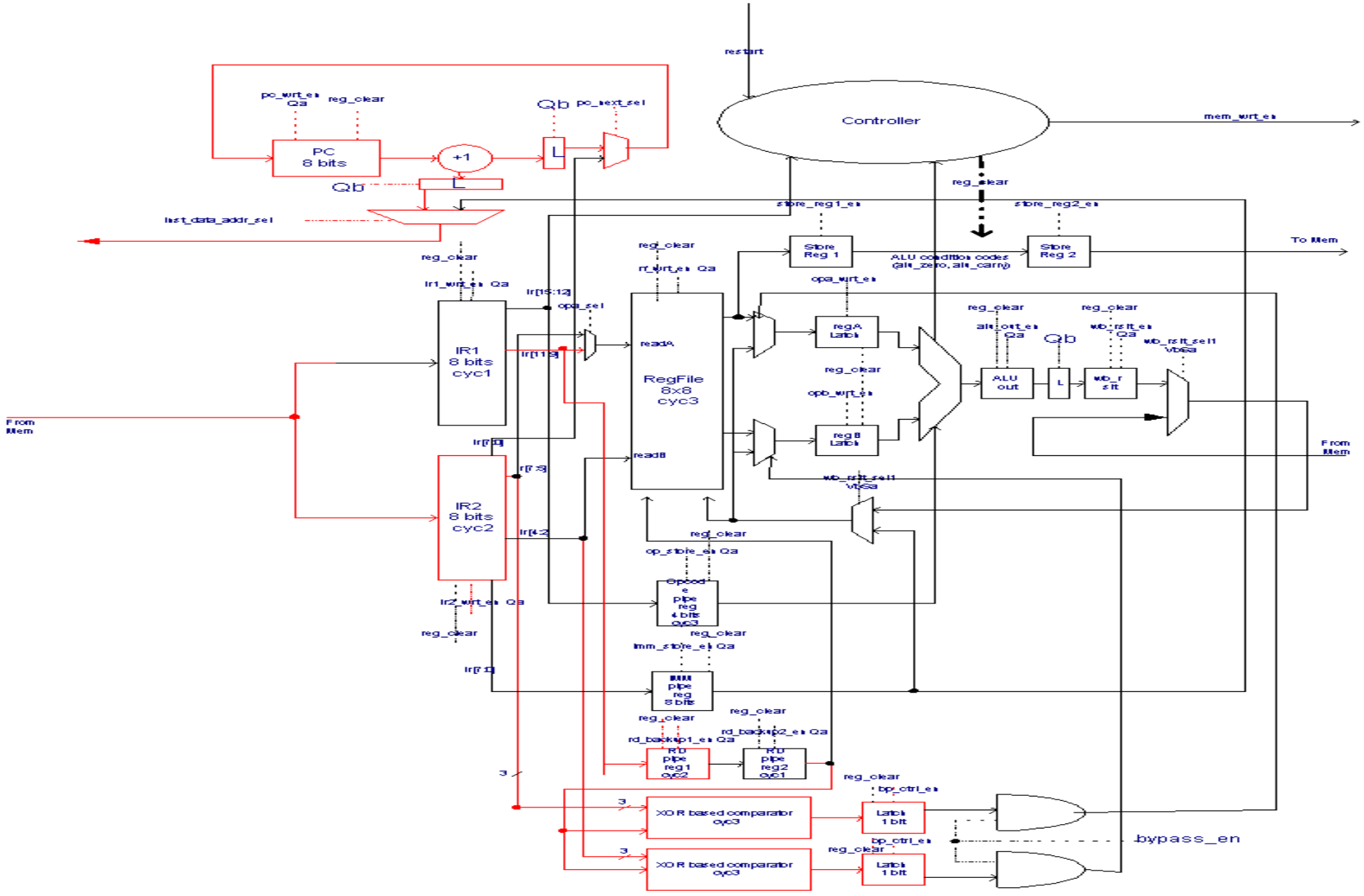
CPU Schematic



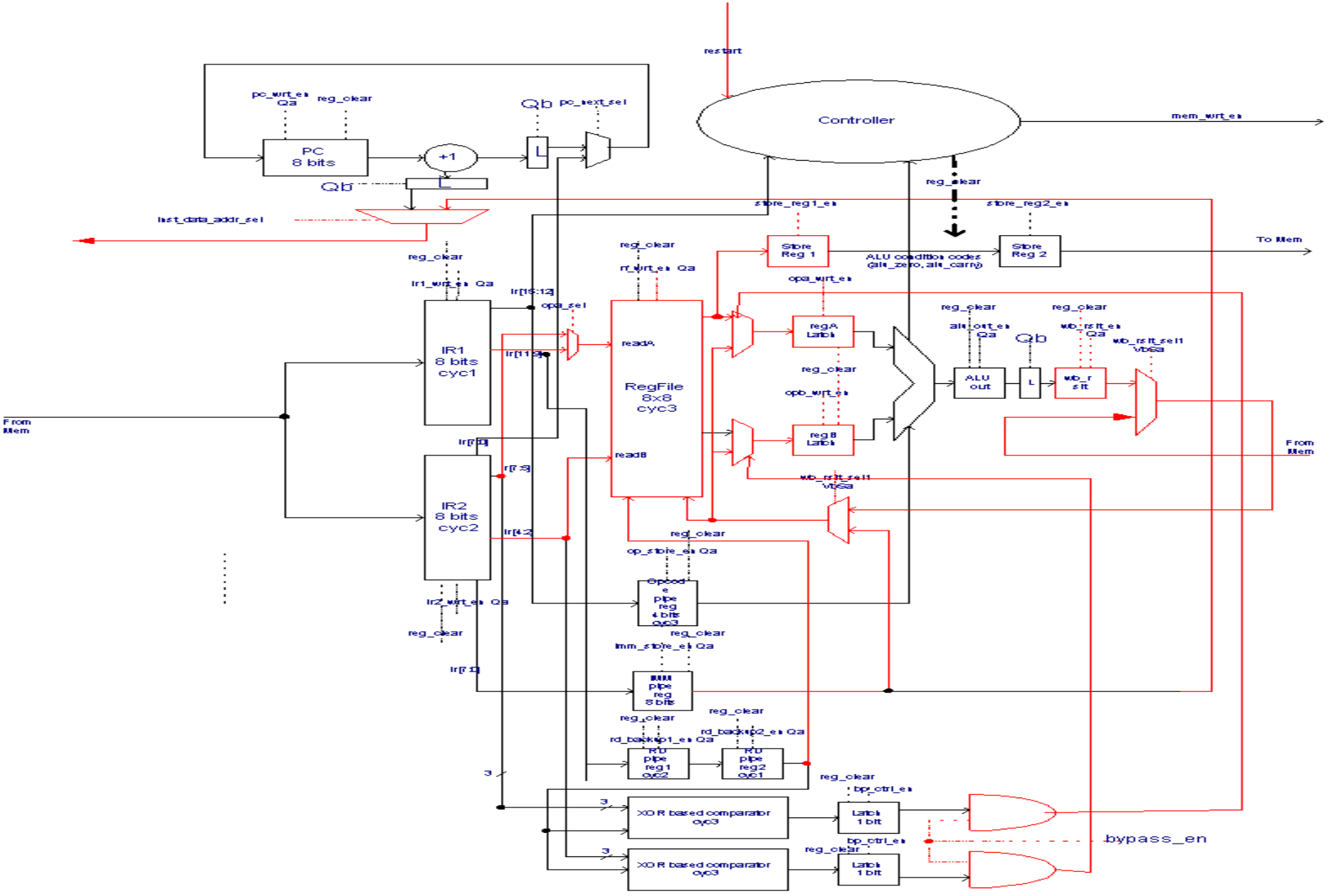
Timing Analysis (1)



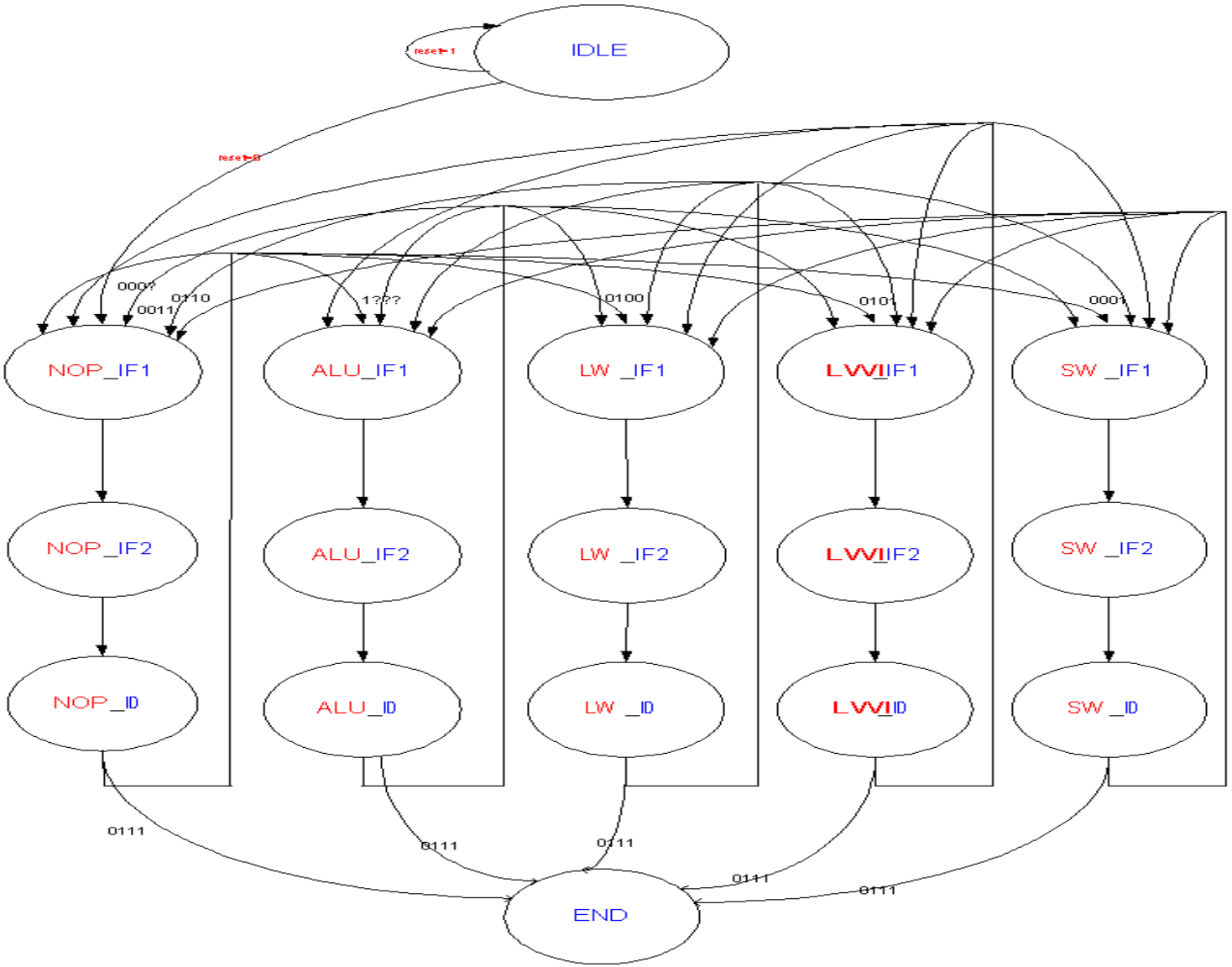
Timing Analysis (2)



Timing Analysis (3)

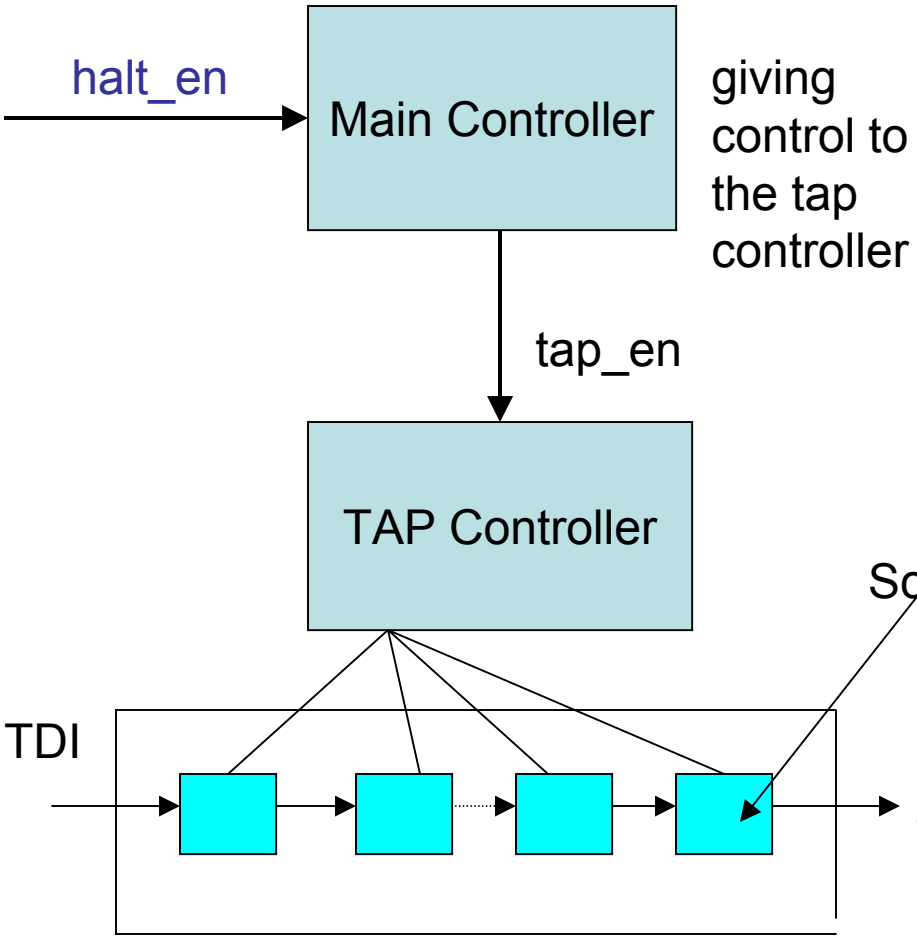


Main PLA

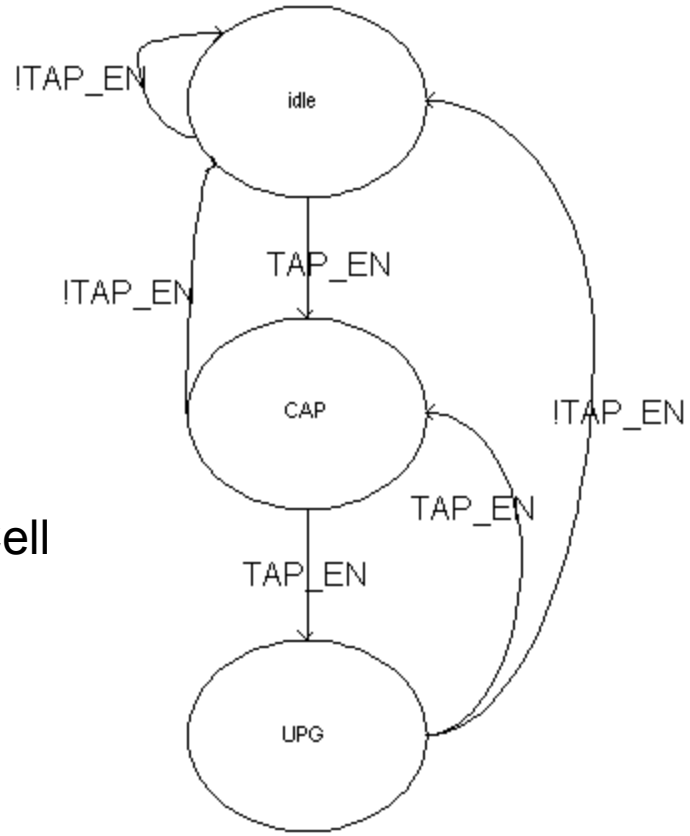


- 8 inputs
- 21 outputs
- 17 states, 5 status bits

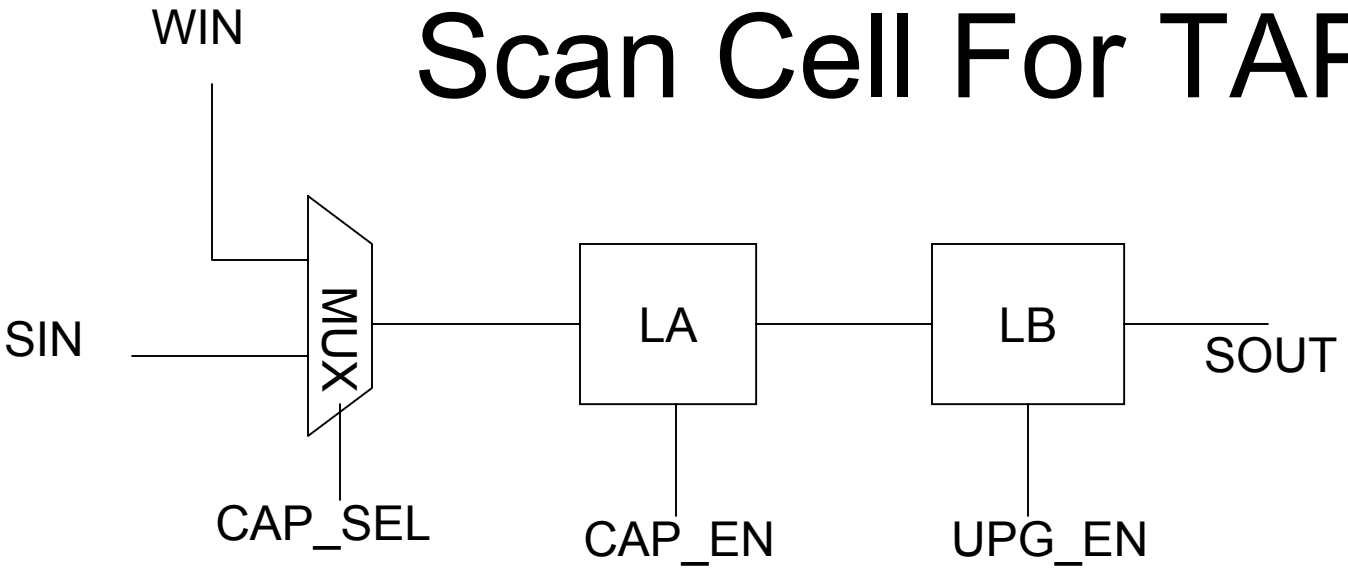
Test Access Port Controller – for CPU Debugging

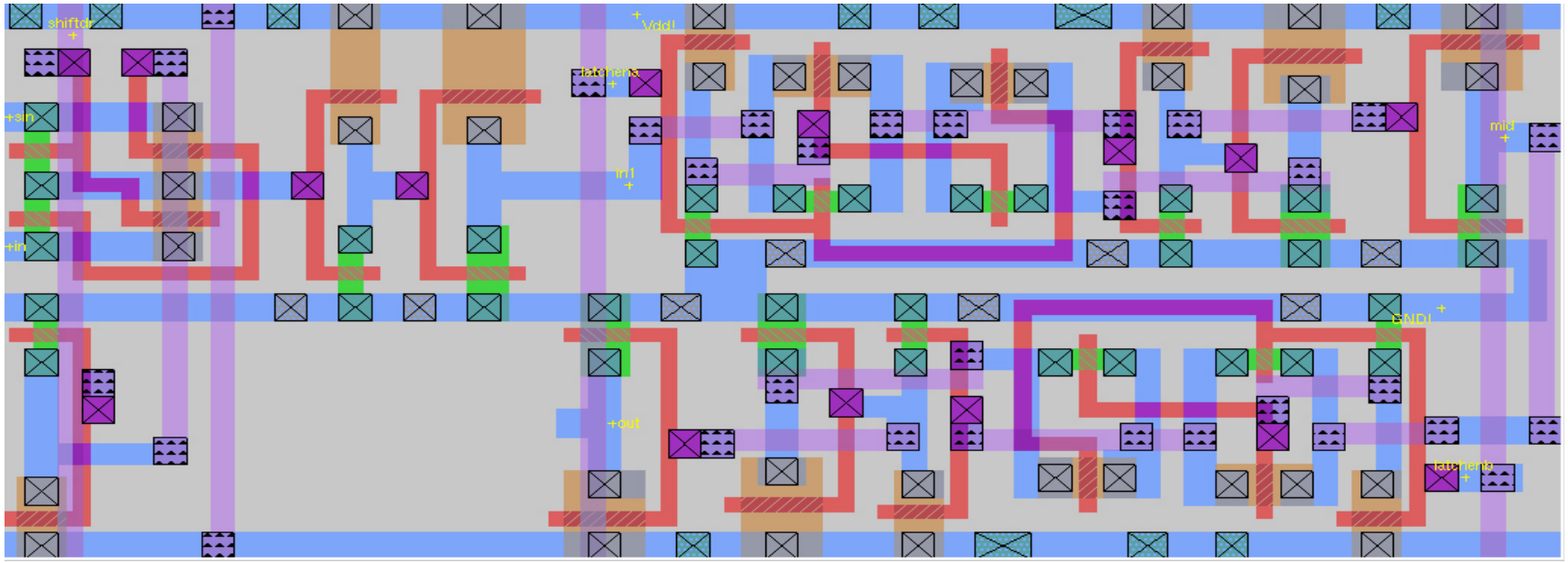


State diagram for TAP

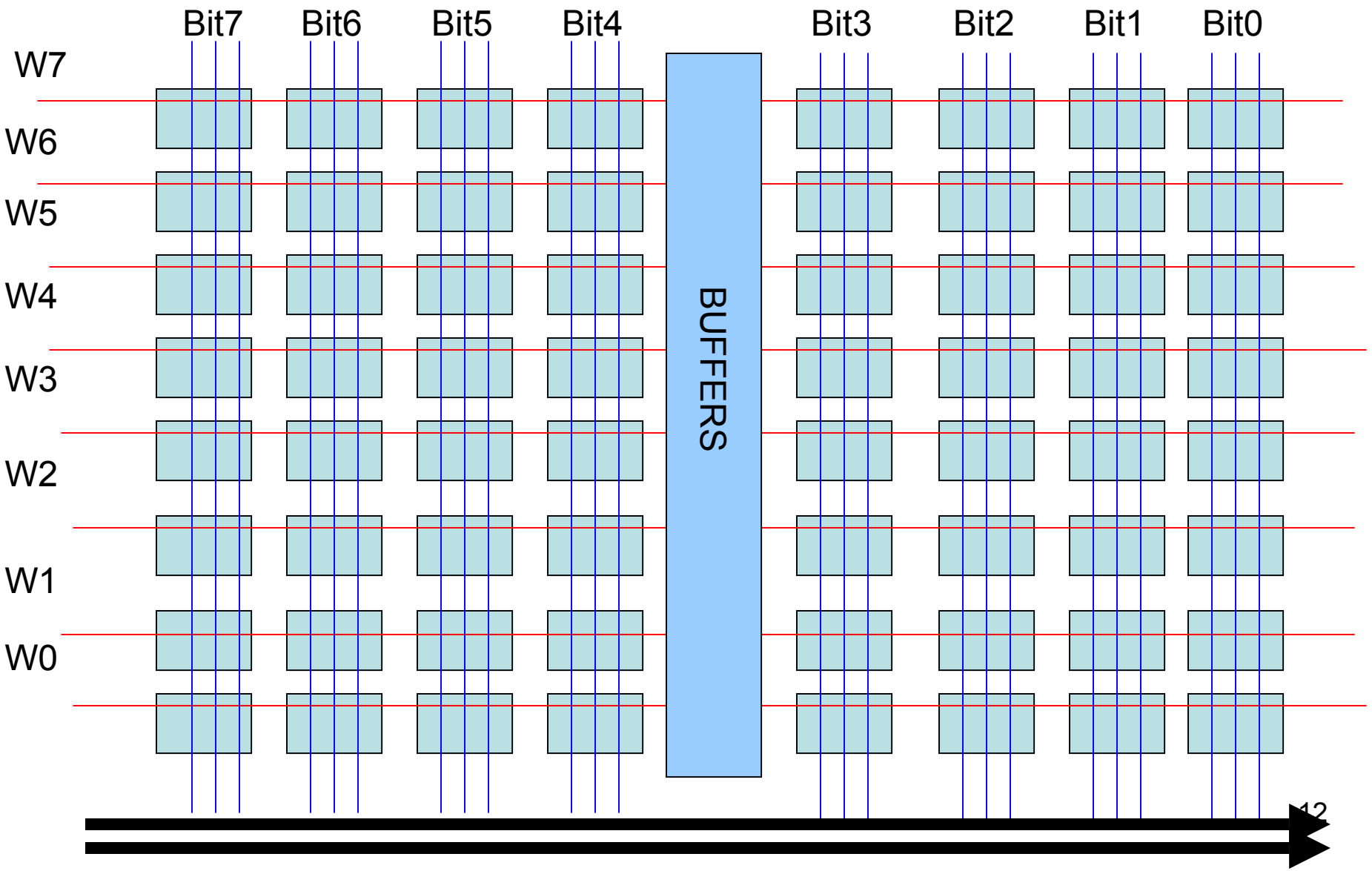


Scan Cell For TAP

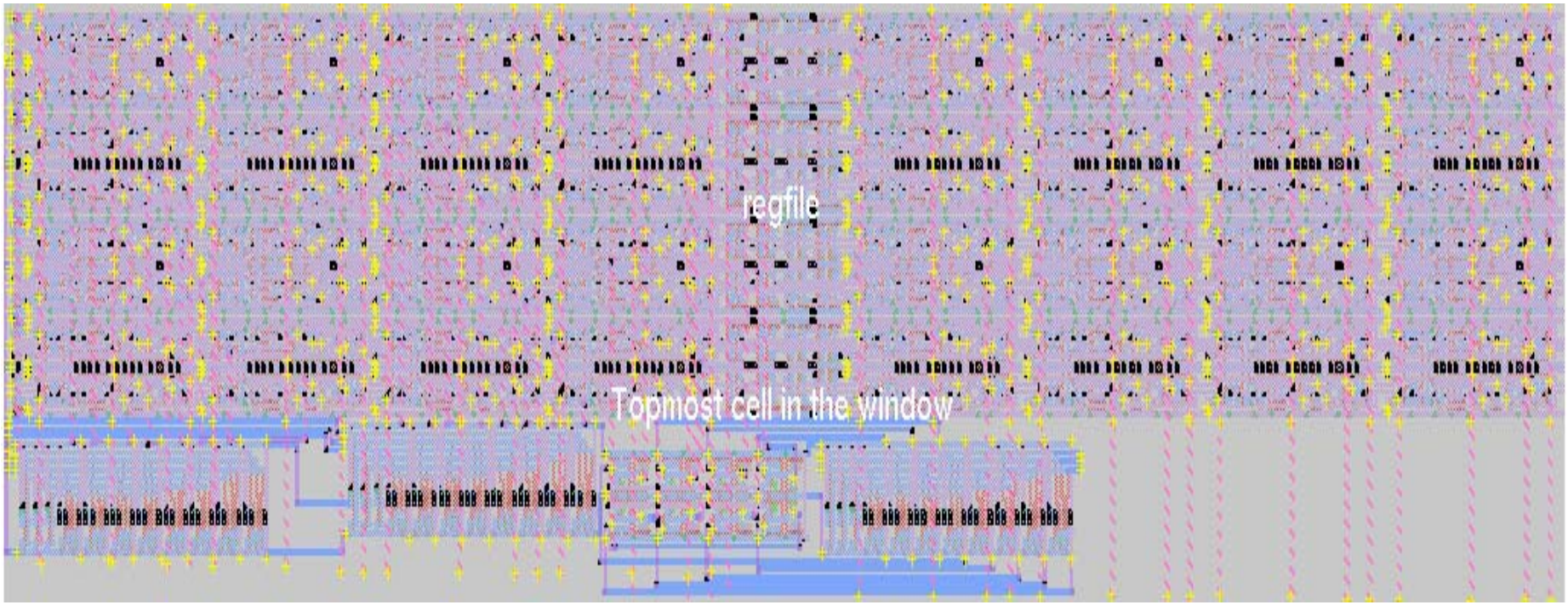




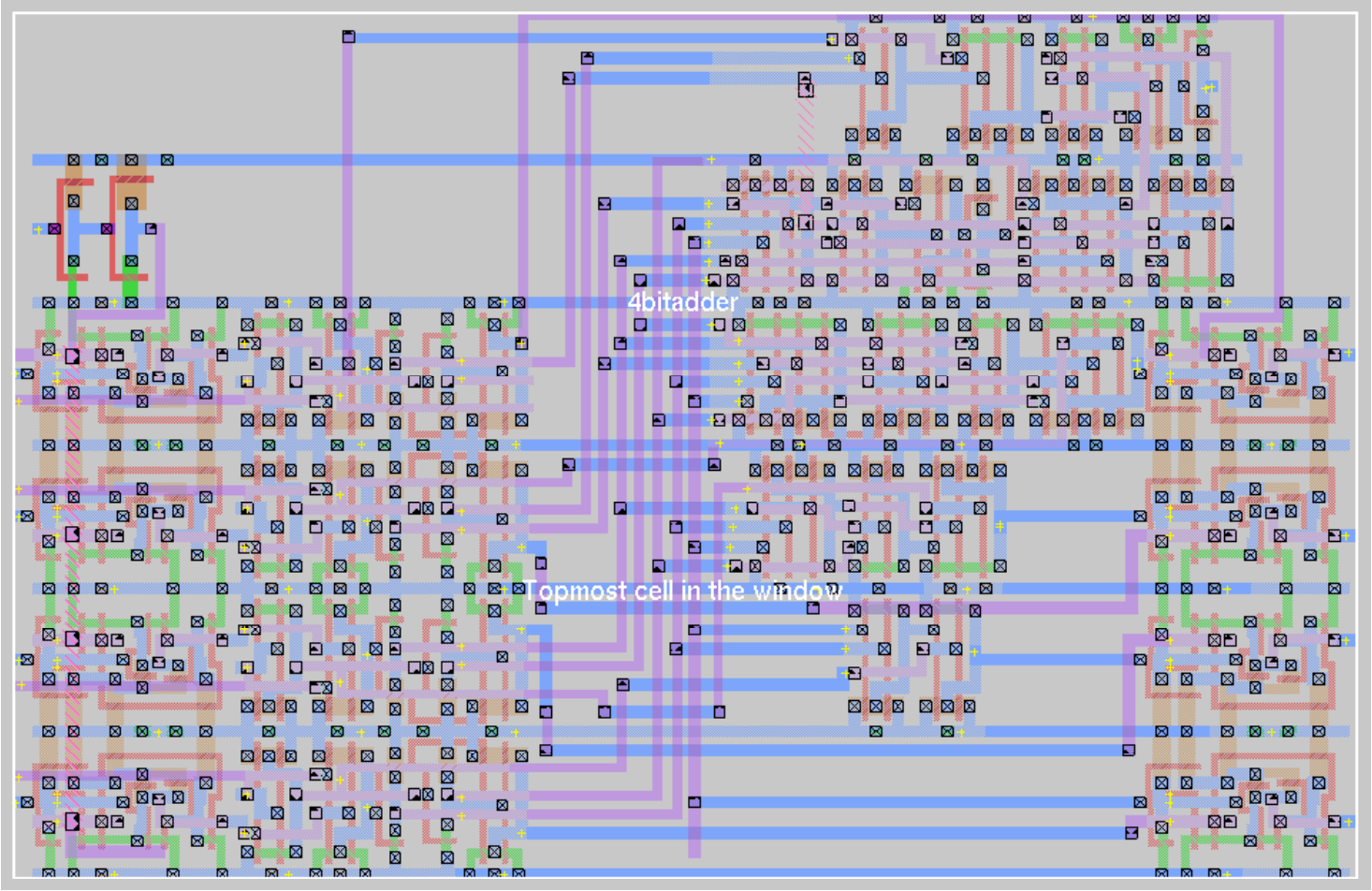
Register File



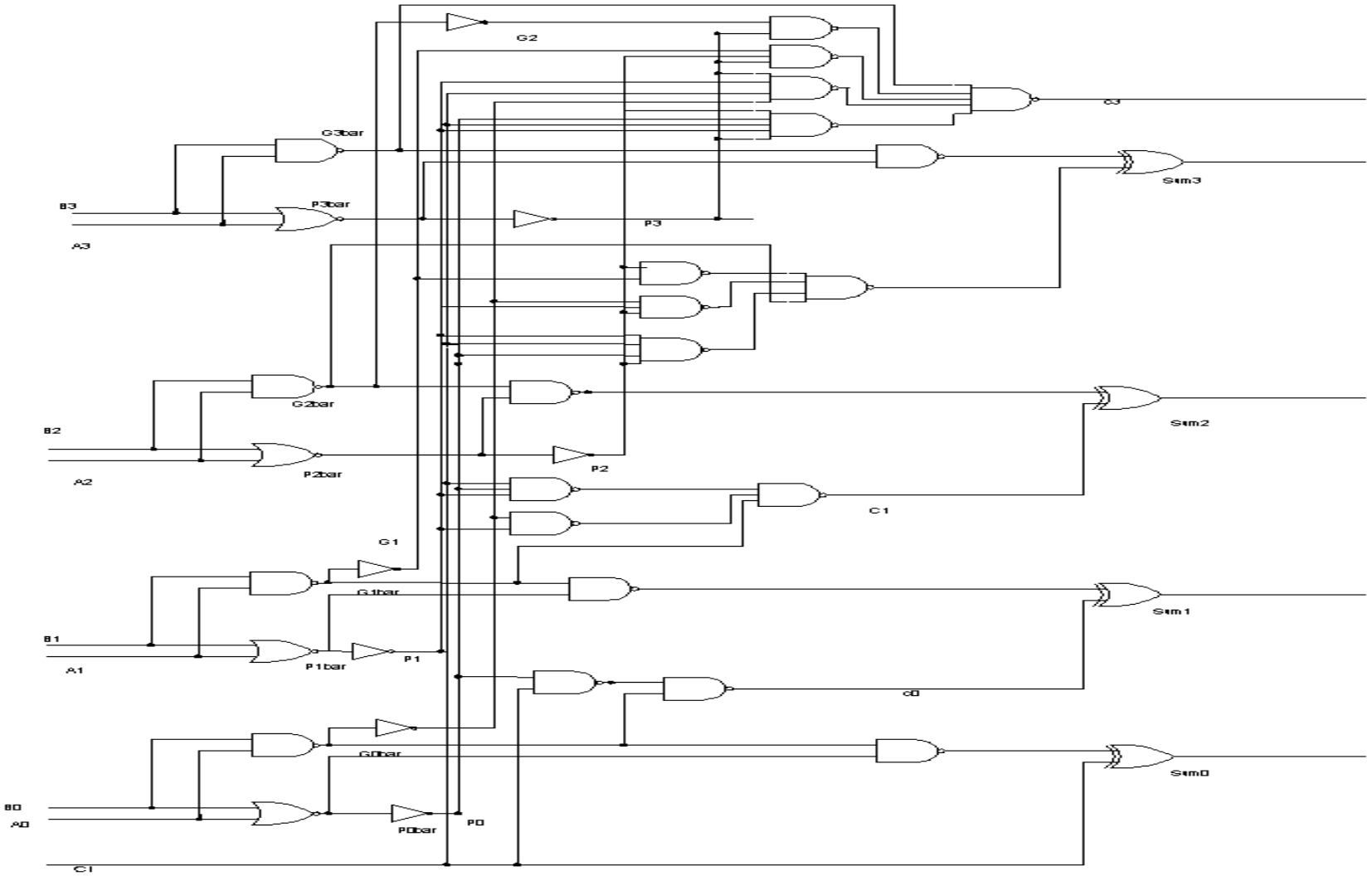
Register File



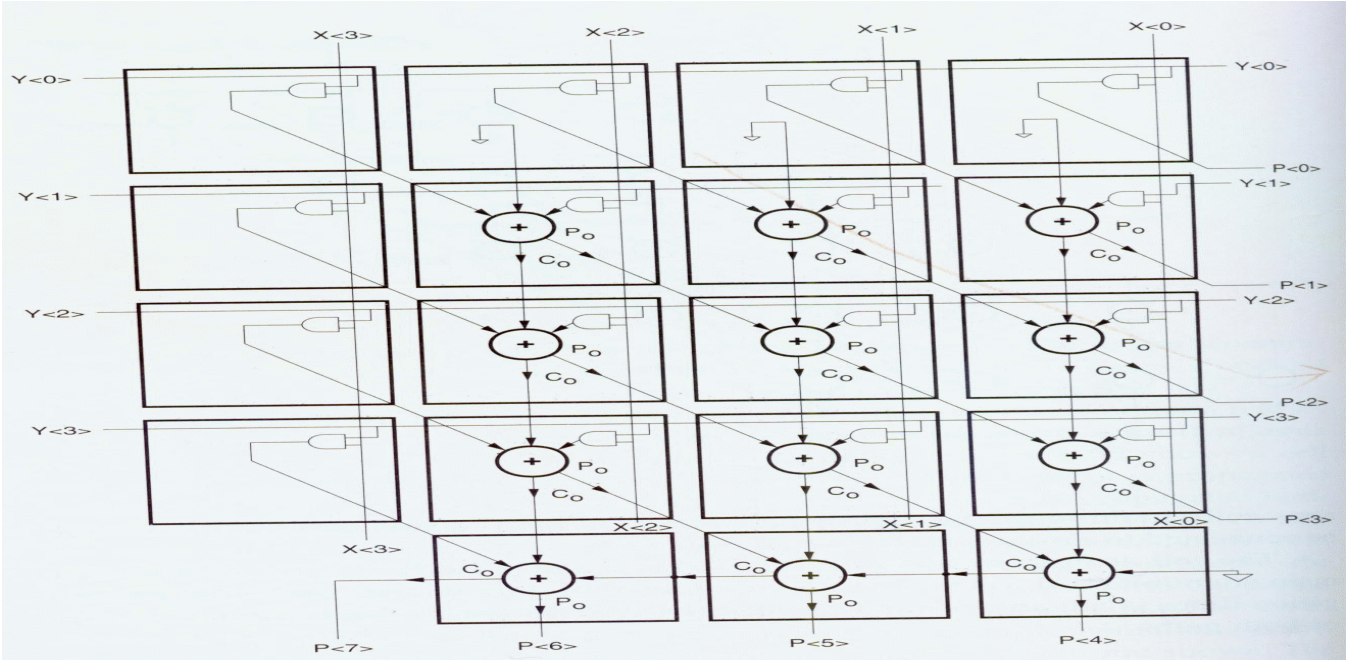
Carry Look-Ahead Adder

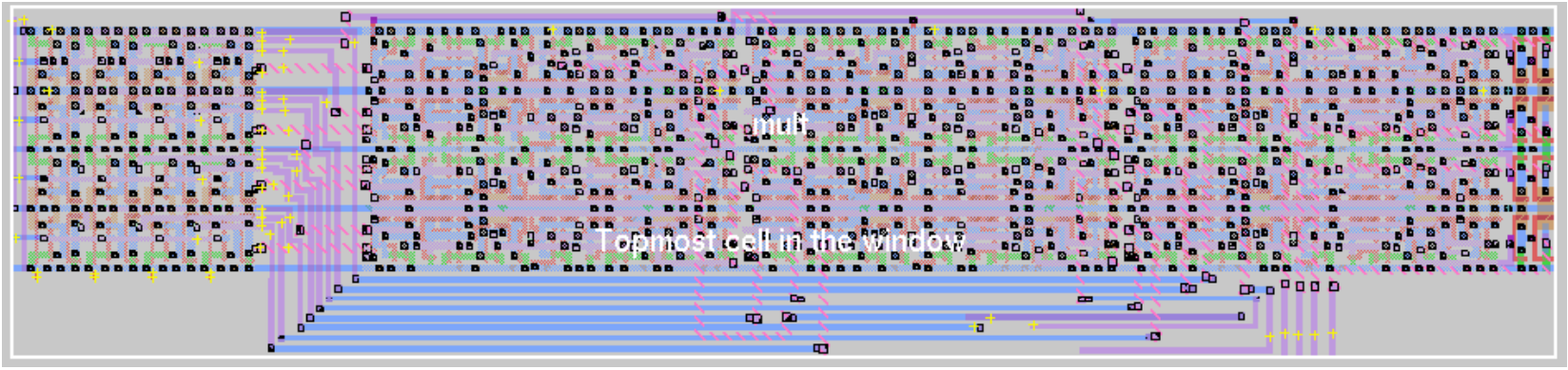


Carry Look-Ahead Adder

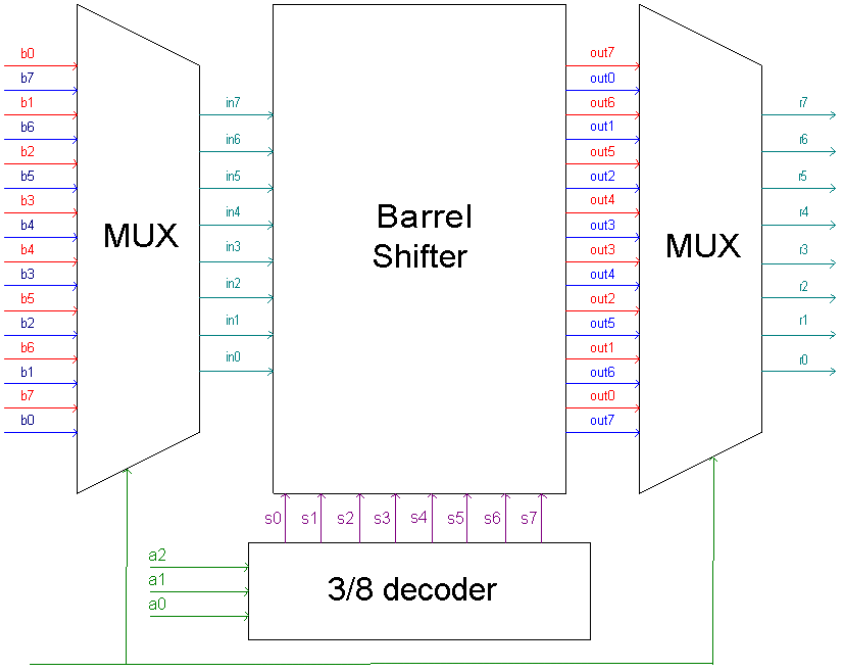


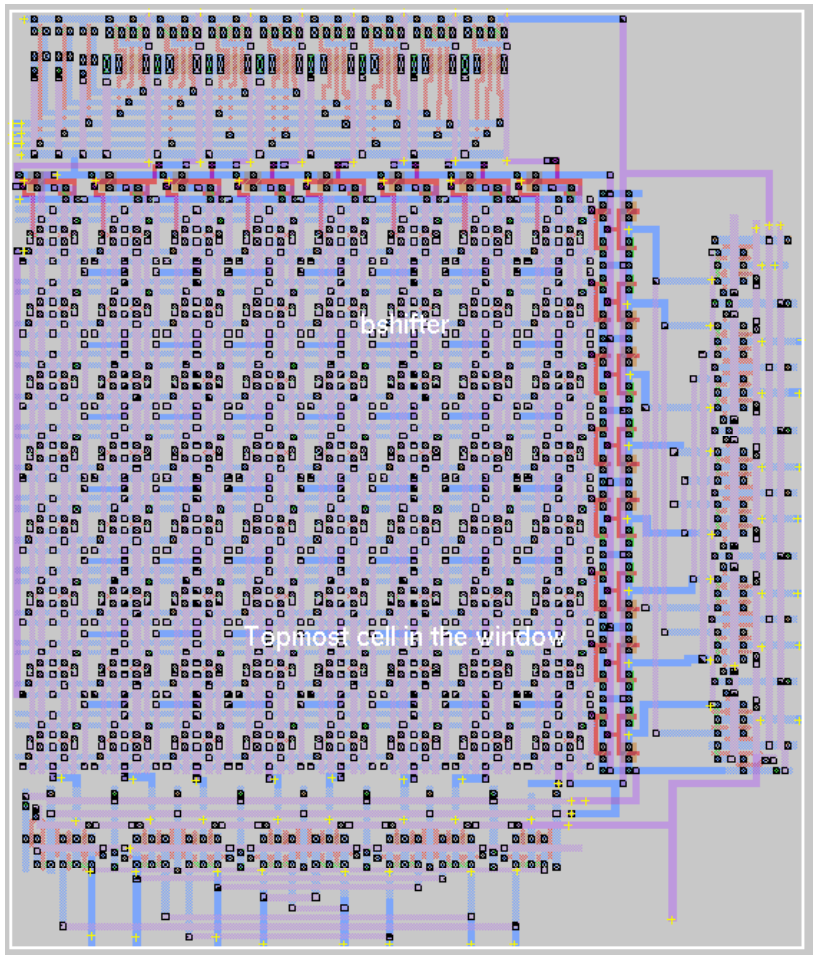
Multiplier


X<3>
X<2>
X<1>
X<0>
Y<0>
Y<1>
Y<2>
Y<3>
P<0>
P<1>
P<2>
P<3>
P<4>
P<5>
P<6>
P<7>
Po
Co

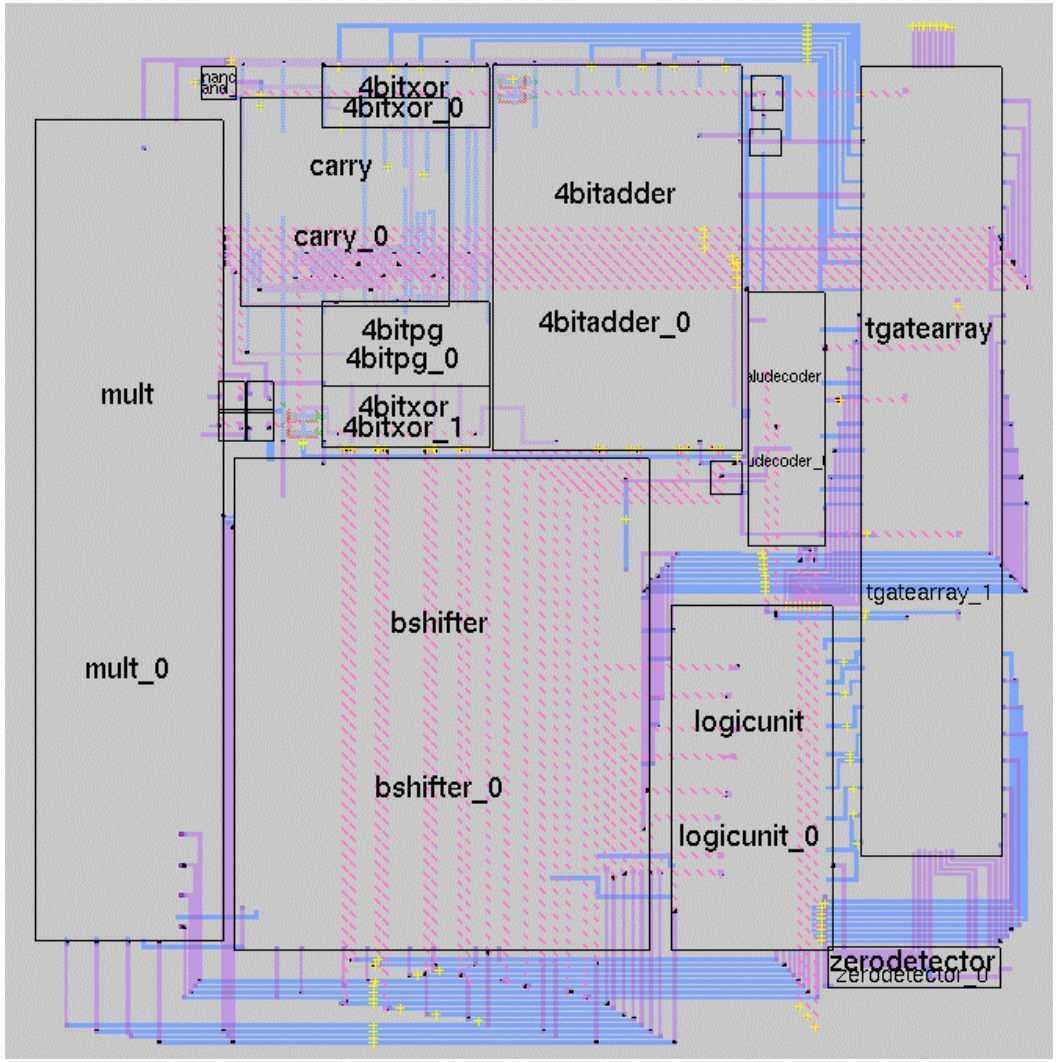

Topmost cell in the window

Barrel Shifter

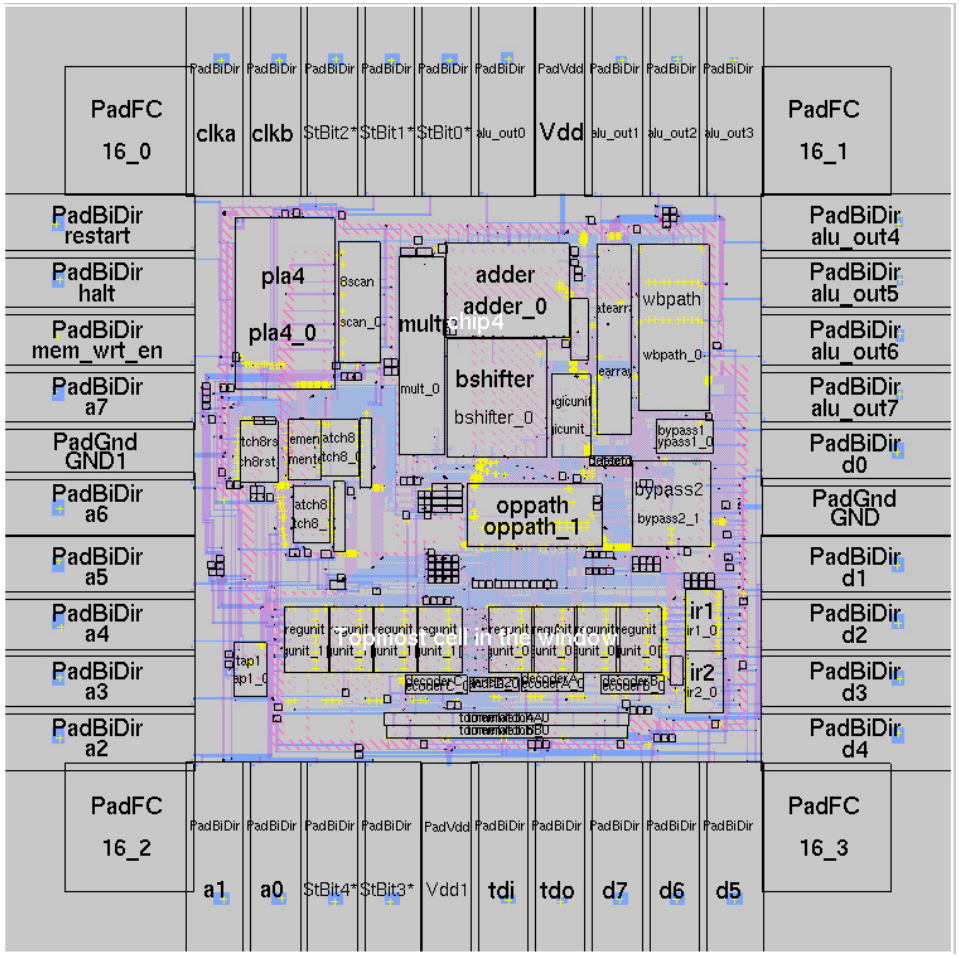




ALU


4bitxor
4bitxor_0
carry
carry_0
4bitadder
4bitadder_0
4bitpg
4bitpg_0
4bitxor
4bitxor_1
mult
mult_0
bshifter
bshifter_0
tgatearray
tgatearray_1
logicunit
logicunit_0
zerodetector

Floor Plan


PadFC 16_0
clka
clkb
StBit2*
StBit1*
StBit0*
alu_out0
Vdd
alu_out1
alu_out2
alu_out3
PadFC 16_1
PadBiDir restart
PadBiDir halt
PadBiDir mem_wrt_en
PadBiDir a7
PadGnd GND1
PadBiDir a6
PadBiDir a5
PadBiDir a4
PadBiDir a3
PadBiDir a2
PadBiDir alu_out4
PadBiDir alu_out5
PadBiDir alu_out6
PadBiDir alu_out7
PadBiDir d0
PadGnd GND
PadBiDir d1
PadBiDir d2
PadBiDir d3
PadBiDir d4
PadFC 16_2
a1
a0
StBit4*
StBit3*
Vdd1
tdi
tdo
d7
d6
d5
PadFC 16_3
pla4
pla4_0
adder
adder_0
bshifter
bshifter_0
wbpath
wbpath_0
oppath
oppath_1
bypass2
bypass2_1
ir1
ir2
Topmost cell in the window

IRSIM Test Code Sequences

We have four testing code sequences

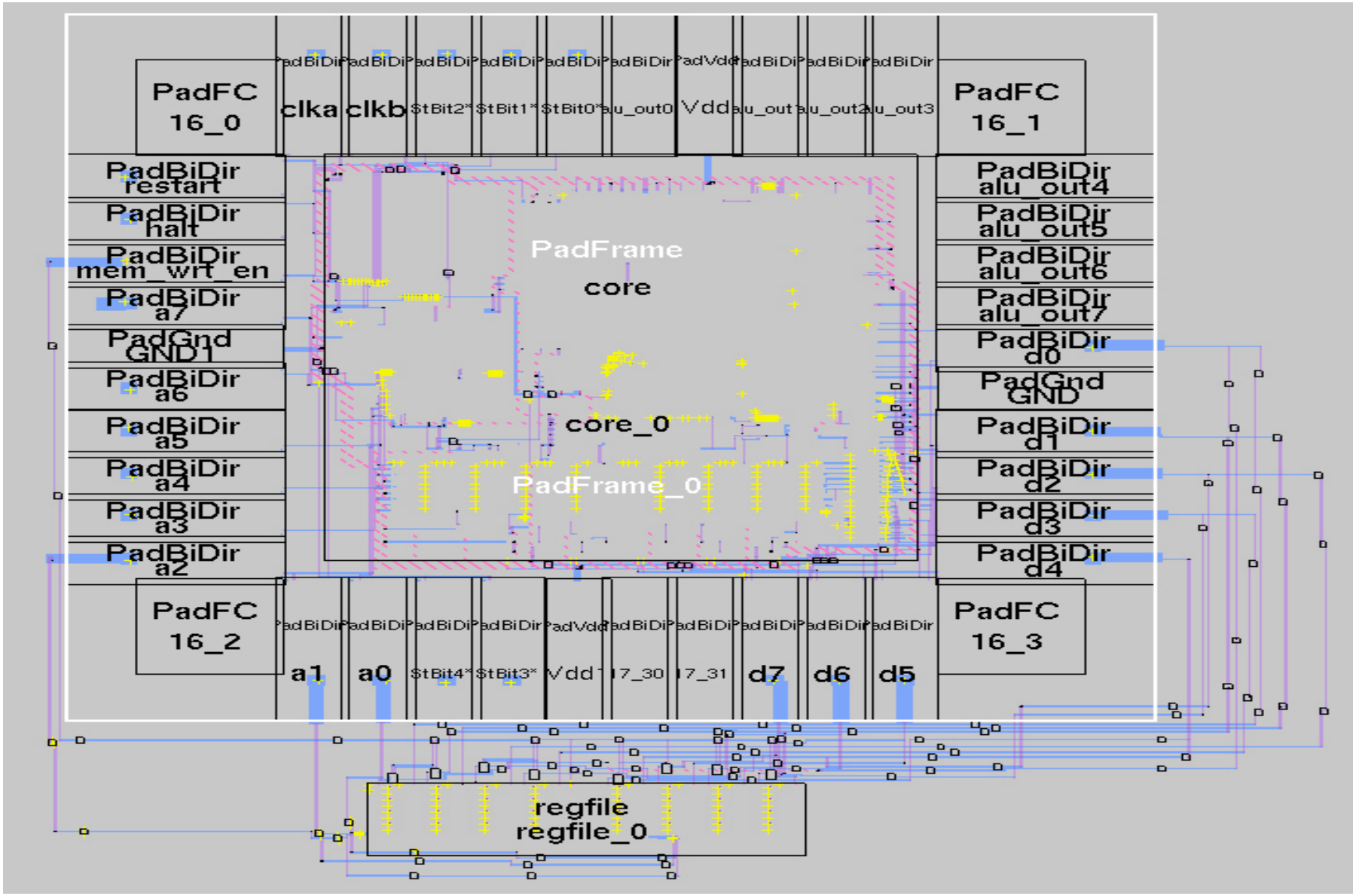
```
LW R0 #129;
LW R1 #130;
ADD R0 R1 R0;
ADD R0 R0 R1;
JC #114;
```

```
LW R4 #168;
LWI R5 #3;
MULT R4 R4 R5;
STORE R4 #168;
```

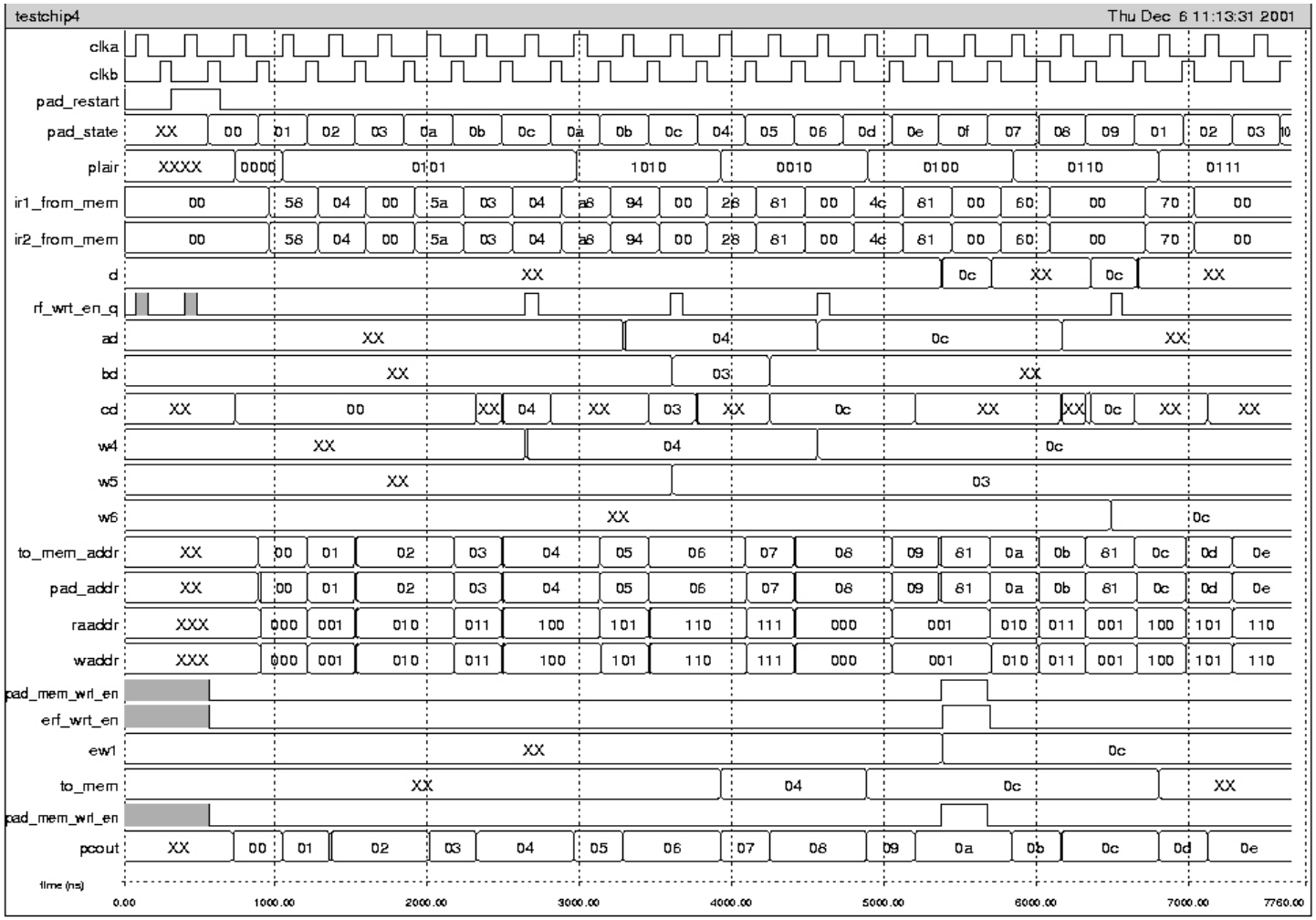
```
LWI R0, #18;
LW R1 #154;
AND R2 R0 R1;
JR #32;
OR R3 R0 R1;
NOT R4 R0;
SLL R5 R0 R1;
SRL R6 R0 R1;
ADD R7 R0 R1;
SW R6 #145;
```

```
LW R2 #129;
LWI R3 #70;
(HALT)
SUB R2 R2 R3;
```

Memory Access Testing



Memory Access Testing Result



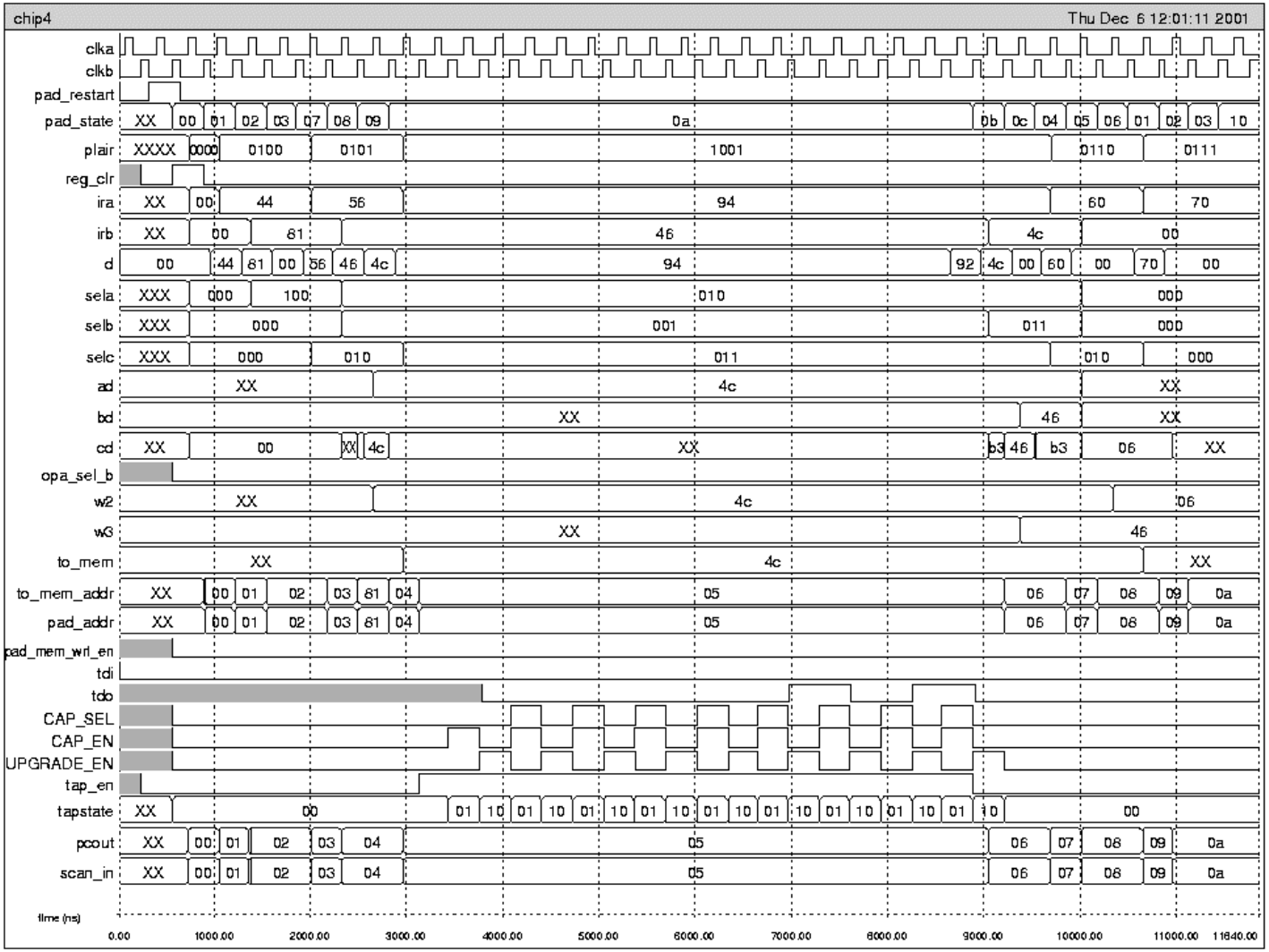
TAP Testing Result

LW R2 #129;

LWI R3 #70;

(HALT)

SUB R2 R2 R3;



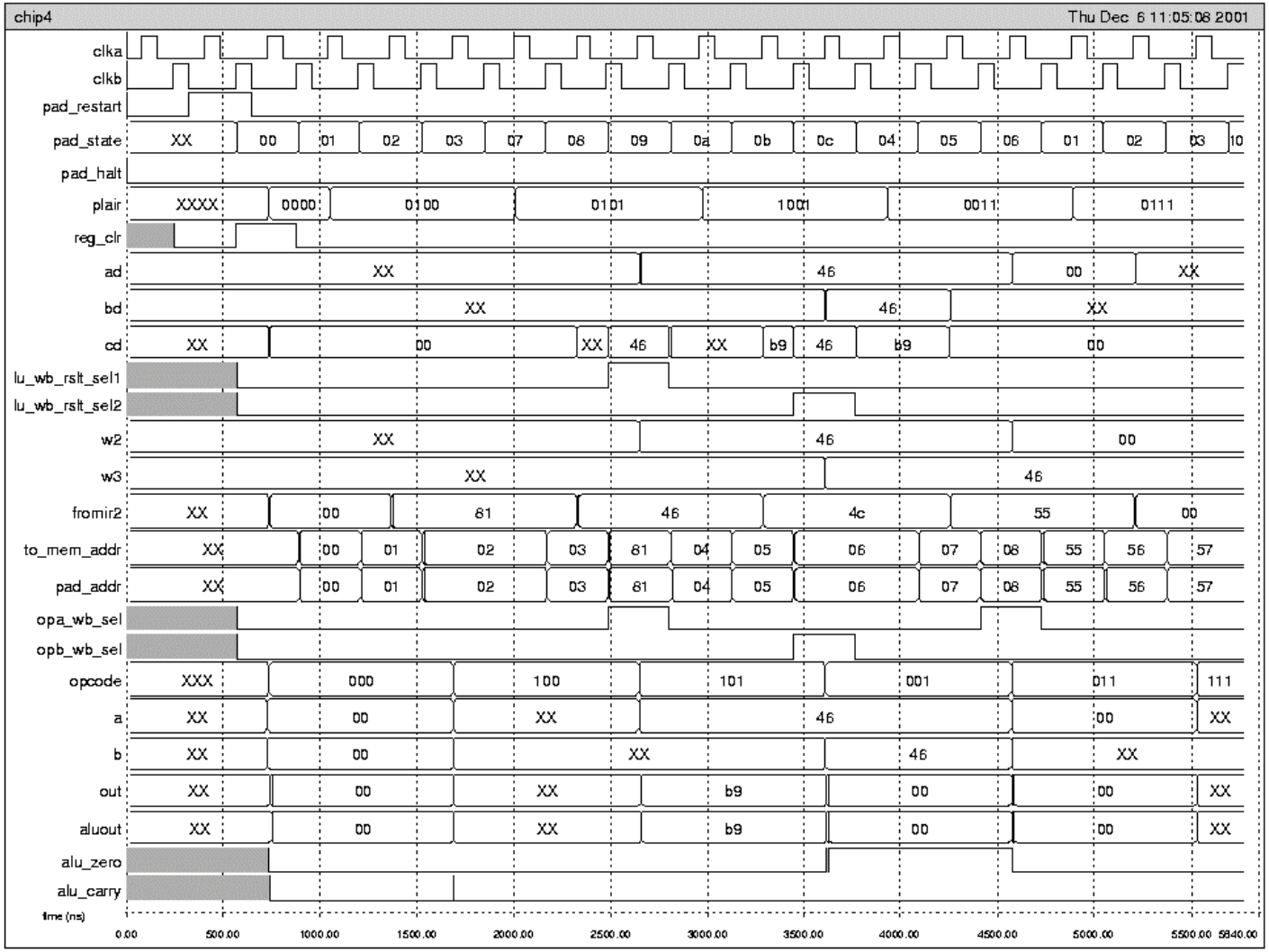
Testing (JZ)

LW R2 #129;

LWI R3 #70;

SUB R2 R2 R3;

JZ #85;



Testing (JC)

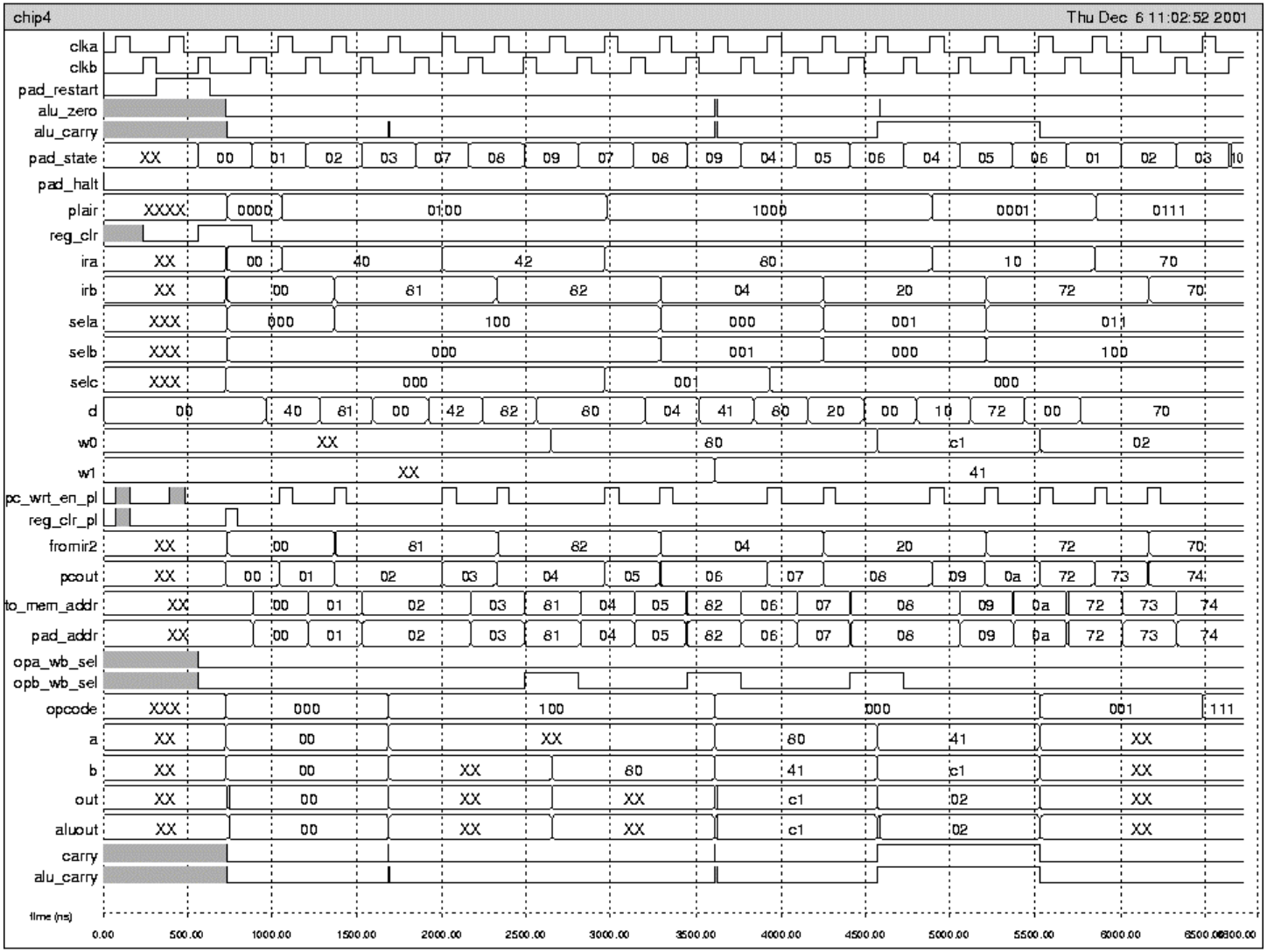
LW R0 #129;

LW R1 #130;

ADD R0 R1 R0;

ADD R0 R0 R1;

JC #114;



General ALU Testing

LWI R0, #18;

LW R1 #154;

AND R2 R0 R1;

JR #32;

OR R3 R0 R1;

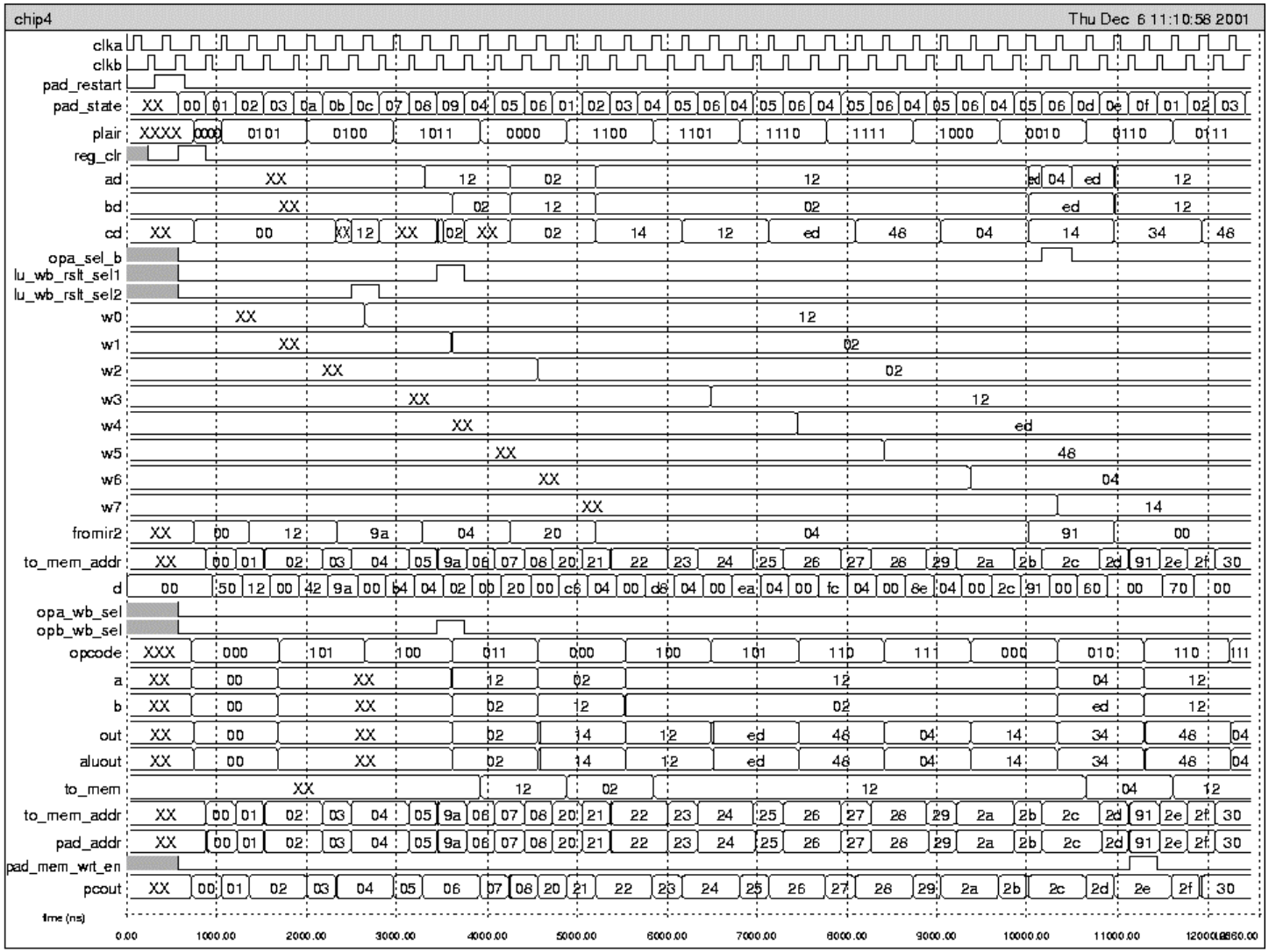
NOT R4 R0;

SLL R5 R0 R1;

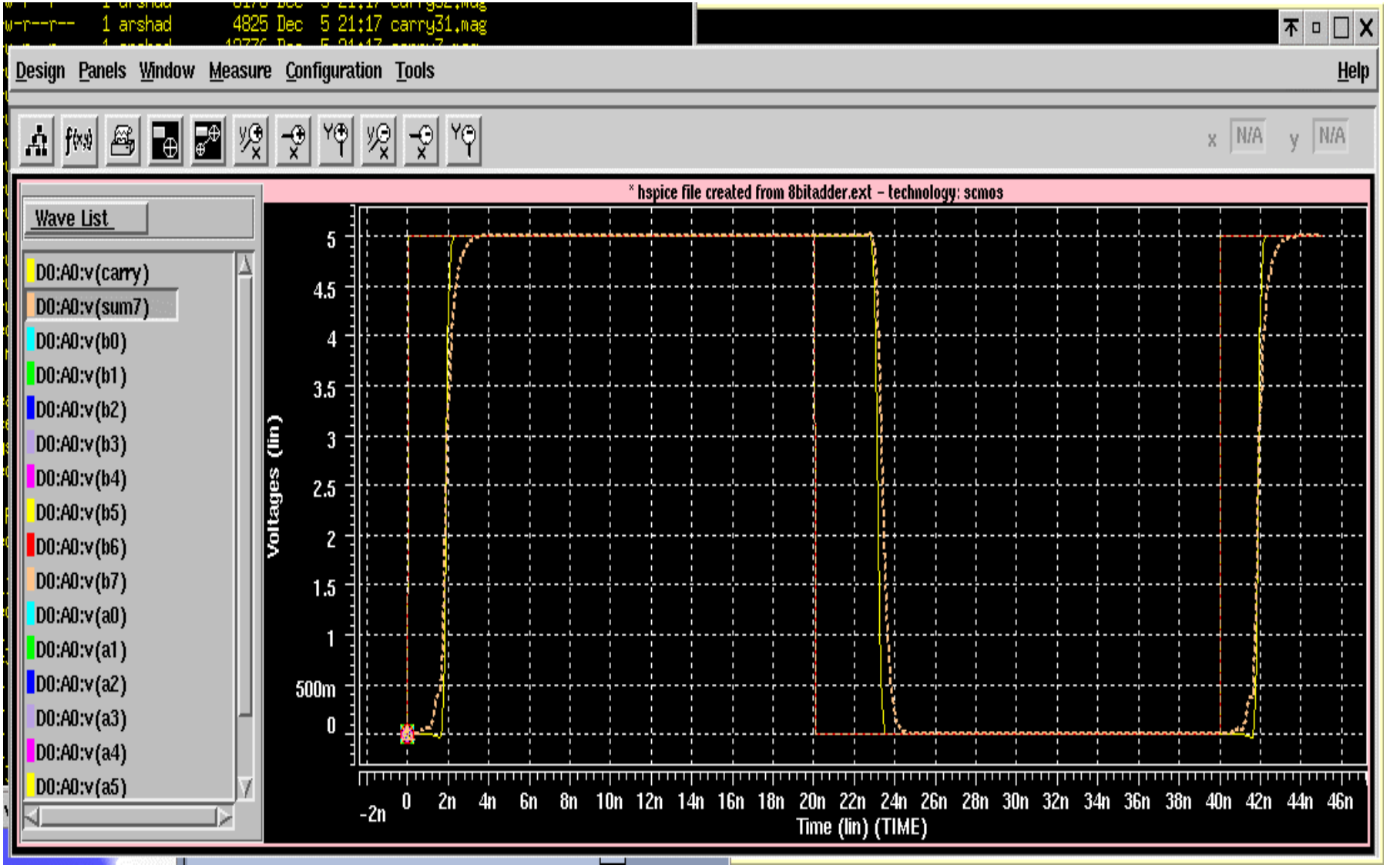
SRL R6 R0 R1;

ADD R7 R0 R1;

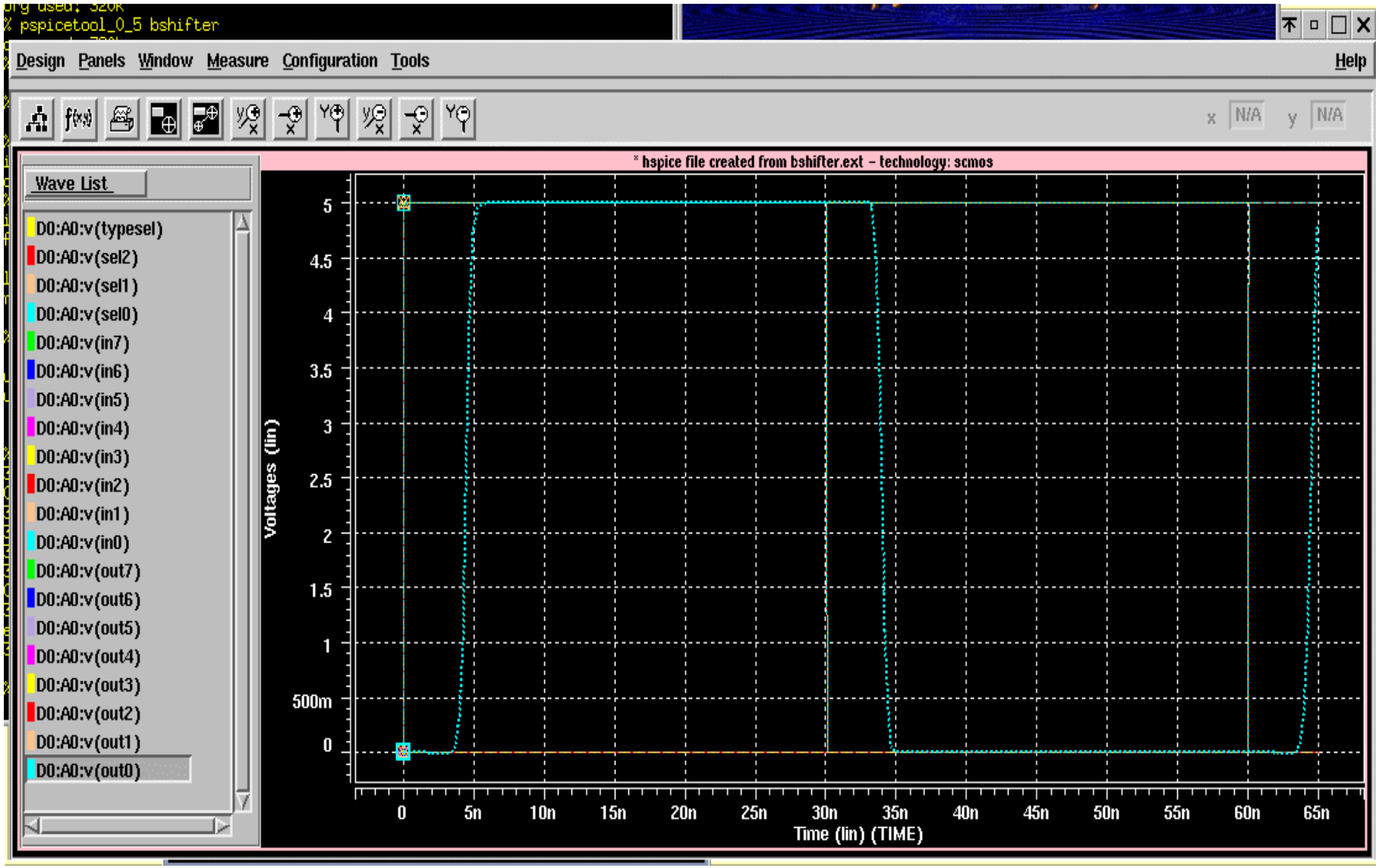
SW R6 #145;



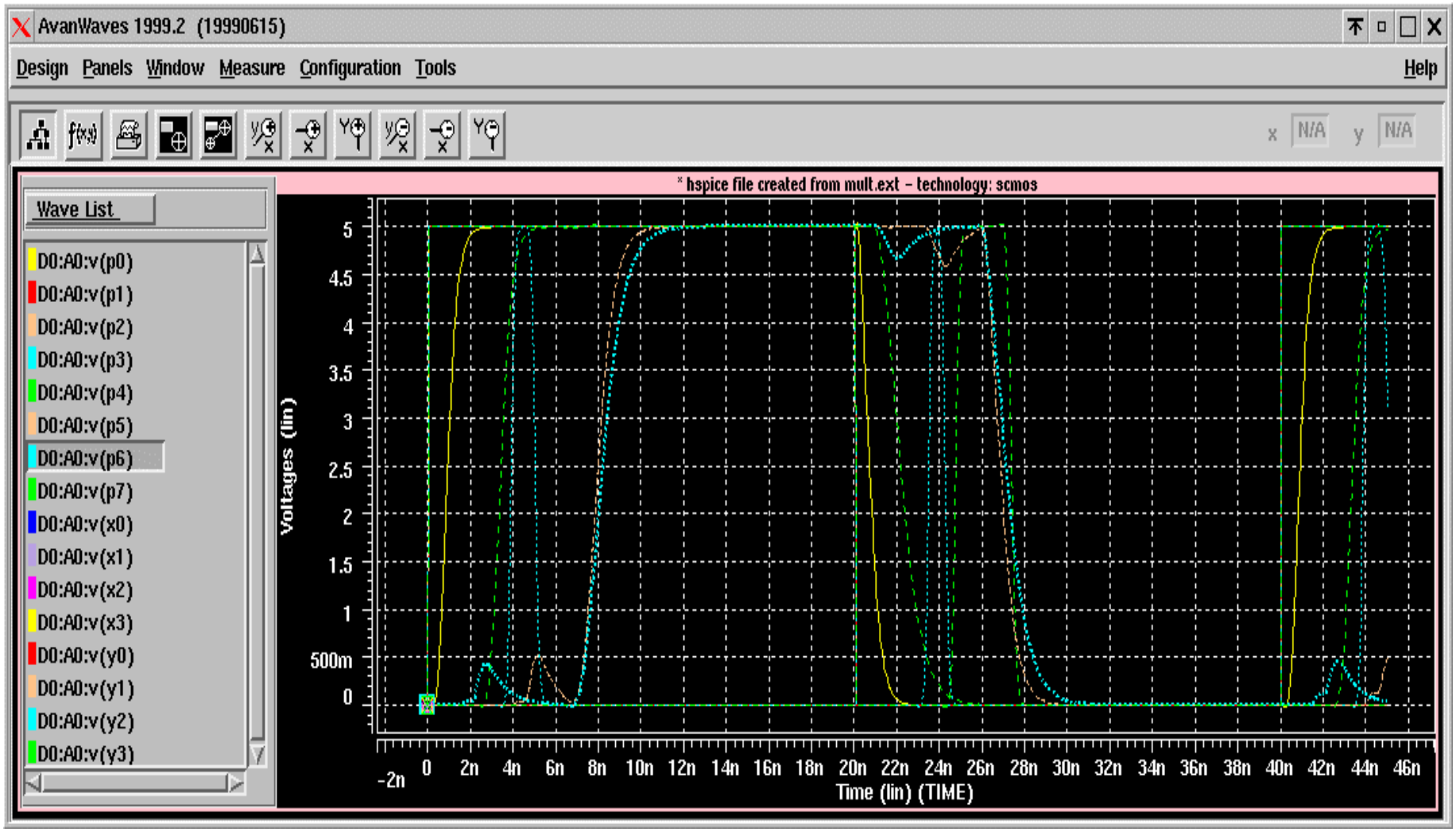
Spice Analysis (Adder)



Spice Analysis (Barrel Shifter)

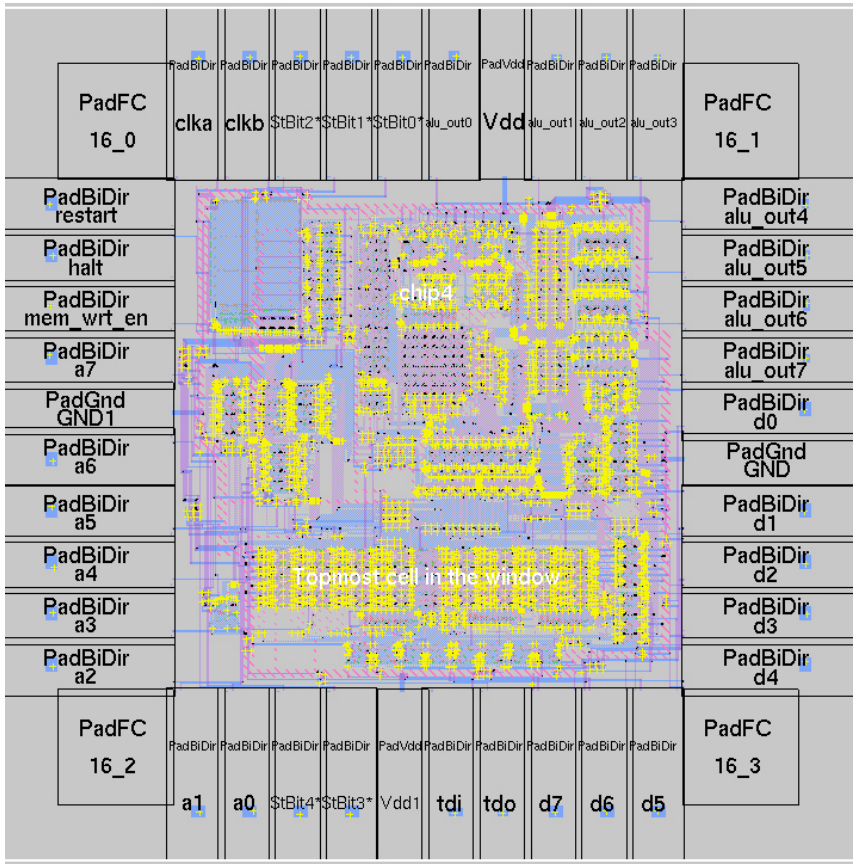


Spice Analysis (Multiplier)



Longest Path Delay: 12ns

Full Chip



Timing Analysis with Crystal and Spice Analysis result:

- The longest path 12ns delay VbSa signal through 4x4 multiplier
- Smallest clock cycle period 24ns for pipeline.
- Max frequency 42 MHz.
- 8500 transistors (excluding the pad frame)

What We Have Learned

- Coordination and cooperation!
- Always keep yourself on schedule!
- Learn fast and apply what you learn fast!

The End

Go, Elec422!
Go, AMD!