Rice University
Elec 422
VLSI Design I

Magic Editor Tutorial

- **Building of Basic Inverter**
- **Addition of Substrate Contacts**
- **Node Labels**

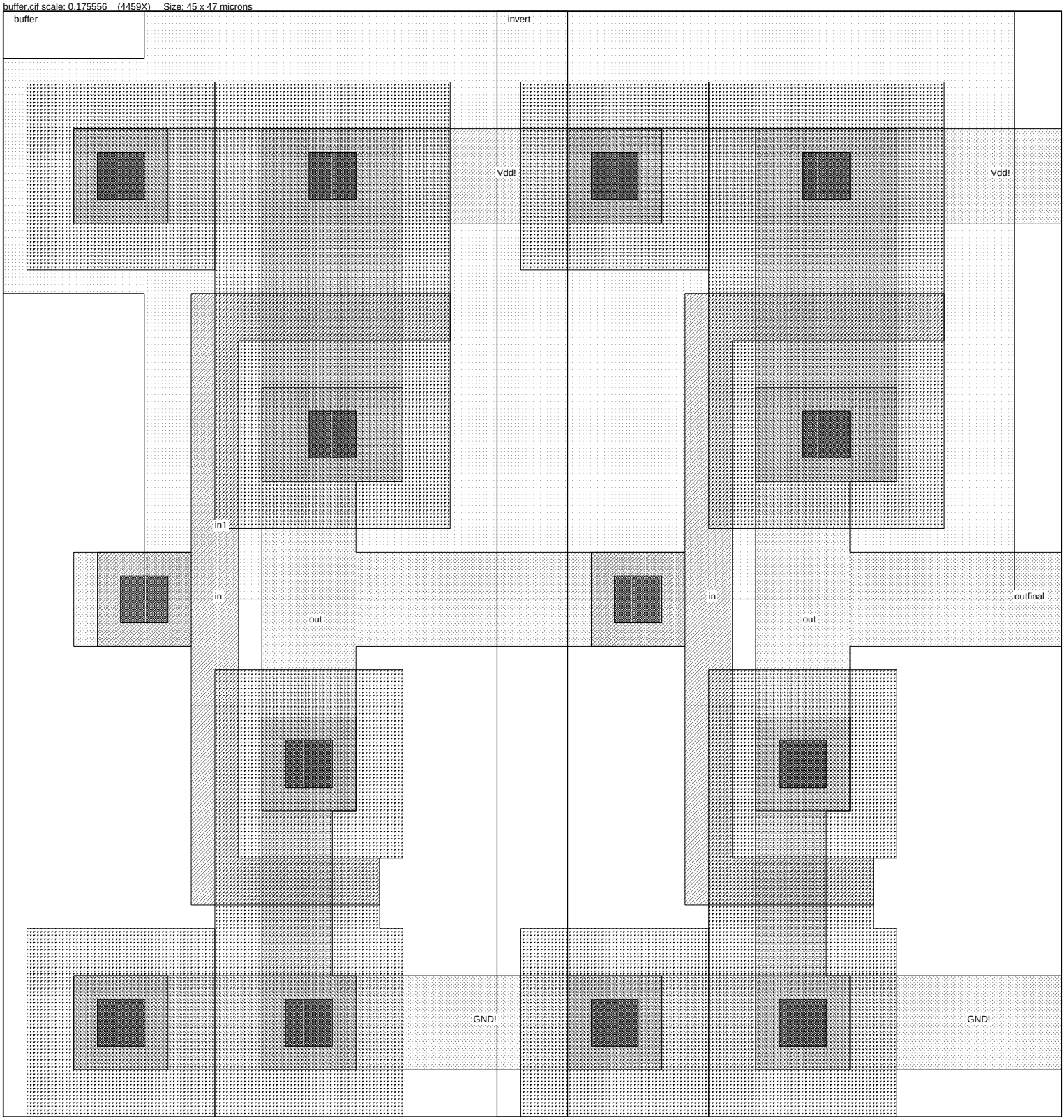
Inverter Replication

- **Buffer Cell Contains Two Inverters**
- **Using Getcell Command**
- **Top-Level Cell Labels**

Circuit / CIF Extraction

- **:extract Within Magic**
- **:cif Within Magic**

buffer.cif scale: 0.175556 (4459X) Size: 45 x 47 microns



Final Circuit Extraction

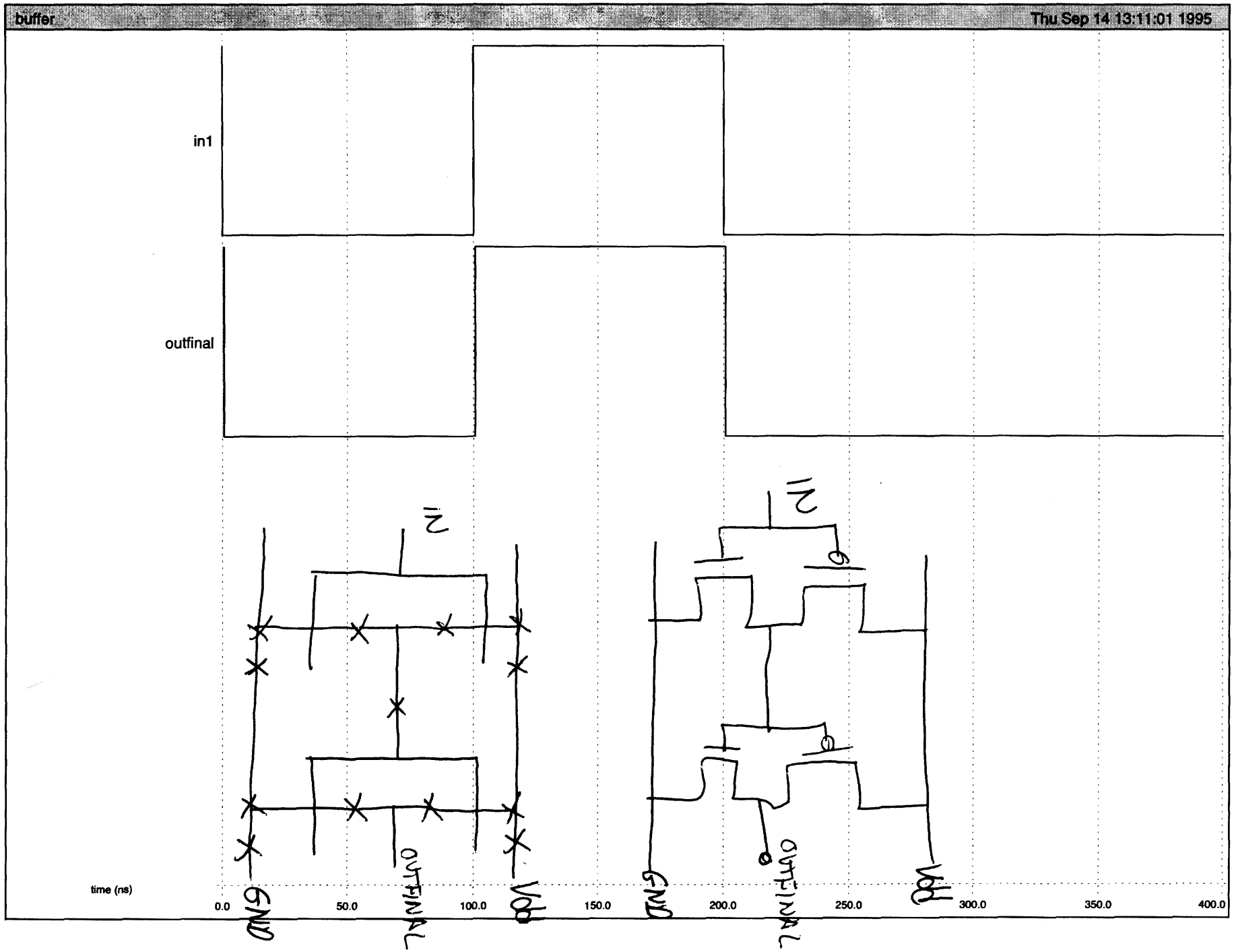
- **Ext2sim**
- **Viewing .sim File**
- **Checking Node Connectivity**

IRSIM Simulation

- **Creation of .cmd Command File**
- **Loading .sim Netlist File**
- **Loading .cmd File**
- **Printing Simulation Output**

CIF Plotting

- **Pplot or cifplot of CIF File**
- **View Postscript with Ghostview**


buffer
Thu Sep 14 13:11:01 1995
in1
outfinal
time (ns)
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
IN
GND
OUTFINAL
Vdd
IN
GND
OUTFINAL
Vdd

*** buffer.mag ***

```
magic
tech scmos
timestamp 811101482
<< polysilicon >>
rect -25 10 -23 12
<< metal1 >>
rect 8 6 12 10
use invert invert_0
timestamp 811101015
transform 1 0 -25 0 1 -10
box -5 -2 16 38
use invert invert_1
timestamp 811101015
transform 1 0 -4 0 1 -10
box -5 -2 16 38
<< labels >>
rlabel metal1 10 8 10 8 7 outfinal
rlabel polysilicon -24 11 -24 11 1 in1
<< end >>
```

*** invert.mag ***

```
magic
tech scmos
timestamp 811101015
<< polysilicon >>
rect 0 29 3 31
rect 9 29 11 31
rect 0 7 2 29
rect 0 5 3 7
rect 6 5 8 7
<< ndiffusion >>
rect 3 7 6 9
rect 3 2 6 5
<< pdiffusion >>
rect 3 31 9 34
rect 3 27 9 29
<< metal1 >>
rect -1 34 3 38
rect 9 34 16 38
rect 3 20 7 23
rect -5 16 -4 20
rect 3 16 16 20
rect 3 13 7 16
rect -1 -2 3 2
rect 7 -2 16 2
<< polycontact >>
rect -4 16 0 20
<< ndcontact >>
rect 3 9 7 13
rect 3 -2 7 2
<< pdcontact >>
rect 3 34 9 38
```

```
rect 3 23 9 27
<< ntransistor >>
rect 3 5 6 7
<< ptransistor >>
rect 3 29 9 31
<< psubstratepcontact >>
rect -5 -2 -1 2
<< nsubstratencontact >>
rect -5 34 -1 38
<< labels >>
rlabel metal1 13 36 13 36 6 Vdd!
rlabel metal1 12 0 12 0 8 GND!
rlabel metal1 5 17 5 17 1 out
rlabel polysilicon 1 18 1 18 1 in
<< end >>


*** buffer.ext ***


timestamp 811101482
version 5.0
tech scmos
scale 1000 1000 150
resistclasses 30000 80000 40000 100 100 50 5000000 5000000
use invert invert_0 1 0 -25 0 1 -10
use invert invert_1 1 0 -4 0 1 -10
node "outfinal" 0 1 8 6 m1 0 0 0 0 0 0 0 0 16 16 0 0 0 0 0 0
node "in1" 30 1 -25 10 p 4 8 0 0 0 0 0 0 0 0 0 0 0 0 0 0
merge "invert_1/in" "invert_0/out" 0 0 0 0 0 0 0 0 0 0 -8 0 0 0 0 0 0
merge "invert_1/Vdd!" "invert_0/Vdd!" 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
merge "invert_0/in" "in1" 0 -4 -8 0 0 0 0 0 0 0 0 0 0 0 0 0 0
merge "invert_1/GND!" "invert_0/GND!" 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
merge "invert_1/out" "outfinal" 0 0 0 0 0 0 0 0 0 -16 -16 0 0 0 0 0 0


*** invert.ext ***


timestamp 811101015
version 5.0
tech scmos
scale 1000 1000 150
resistclasses 30000 80000 40000 100 100 50 5000000 5000000
node "GND!" 178 29 -5 -2 psc 0 0 16 16 25 22 0 0 52 42 0 0 0 0 0 0
node "out" 163 63 3 7 green 0 0 36 24 22 20 0 0 76 46 0 0 0 0 0 0
node "in" 615 11 -4 16 pc 98 94 0 0 0 0 0 0 4 10 0 0 0 0 0 0
node "Vdd!" 134 44 -5 34 nsc 0 0 42 26 16 16 0 0 44 38 0 0 0 0 0 0
fet nfet 3 5 4 6 6 10 "GND!" "in" 4 0 "GND!" 3 0 "out" 3 0
fet pfet 3 29 4 30 12 16 "Vdd!" "in" 4 0 "out" 6 0 "Vdd!" 6 0


*** buffer.sim ***

| units: 150      tech: scmos
p invert_1/in outfinal Vdd 2 6 -1 19
n invert_1/in GND outfinal 2 3 -1 -5
```

```
p in1 invert_1/in Vdd 2 6 -22 19
n in1 GND invert_1/in 2 3 -22 -5
C in1 GND 12
C outfinal GND 64
C invert_1/in GND 74
C Vdd GND 88


*** buffer.cmd ***


| Irsim Test Vector for buffer3

| Watch nodes
ana in1 outfinal

| Since irsim needs a clock while the inverter is a combinational circuit,
| we will use a dummy clock signal just to keep irsim happy.
clock Vdd 1

|  cycle the input node "in" through a sequence of 1s and 0s
V in1  0 1 0 0

| Simulate the circuit for this sequence of inputs
R


*** buffer.cif ***



DS 1 50 2;
9 buffer;
L CWN;
    B 20 8 -34 128;
    B 20 52 -34 58;
L CMF;
    B 16 16 40 32;
L CPG;
    B 8 8 -96 44;
94 outfinal 40 32 CMF;
94 in1 -96 44 CPG;
C 2 R 1 0 T -100 -40;
C 2 R 1 0 T -16 -40;
DF;
DS 2 50 2;
9 invert;
L CWN;
    B 64 8 24 168;
    B 88 40 12 144;
    B 64 52 24 98;
L CMF;
    B 84 16 22 144;
    B 24 16 24 100;
    B 16 12 20 86;
    B 20 16 -10 72;
    B 52 16 38 72;
```

```
    B 16 28 20 50;
    B 84 16 22 0;
L CPG;
    B 44 8 22 120;
    B 8 36 4 98;
    B 24 16 -4 72;
    B 8 36 4 46;
    B 32 8 16 24;
L CAA;
    B 16 16 -12 144;
    B 24 60 24 122;
    B 16 16 20 44;
    B 12 28 18 22;
    B 16 16 -12 0;
    B 16 16 20 0;
L CCA;
    B 8 8 24 144;
    B 8 8 24 100;
    B 8 8 20 44;
    B 8 8 20 0;
L CCA;
    B 8 8 -12 144;
    B 8 8 -12 0;
L CCP;
    B 8 8 -8 72;
L CSN;
    B 32 32 -12 144;
    B 32 32 20 44;
    B 28 12 18 22;
    B 32 32 20 0;
L CSP;
    B 40 76 24 122;
    B 32 32 -12 0;
94 Vdd! 52 144 CMF;
94 GND! 48 0 CMF;
94 out 20 68 CMF;
94 in 4 72 CPG;
DF;
C 1;
End
```