

GP256 Graphics Co-processor

ELEC 422 – VLSI Design I

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Outline

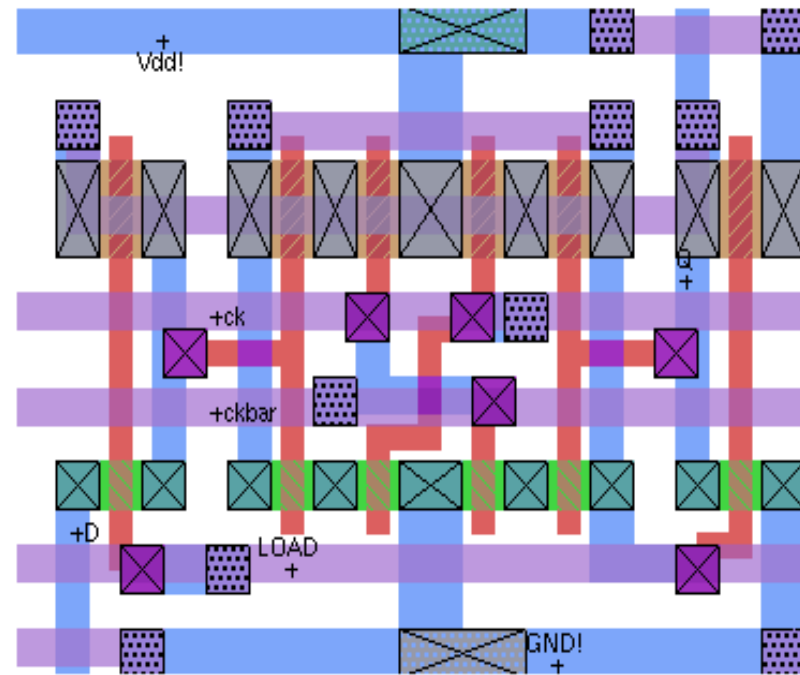
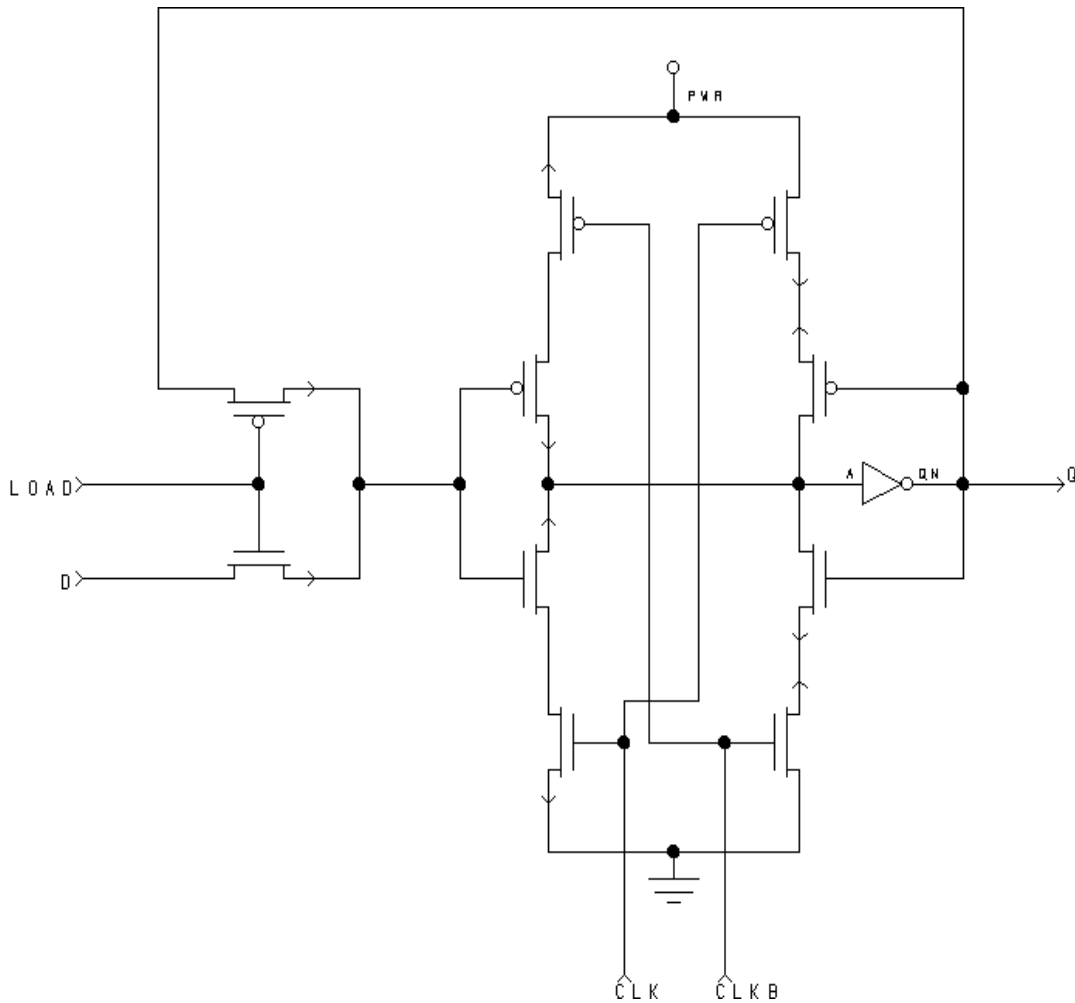
1. Functional Description and Project Status
2. Registers and Multiplexors
3. FSM Controller
4. Address Generation Unit
5. ALU
6. System Performance
7. Floorplan and Cell Hierarchy

Functional Description

- ◆ Graphics Co-Processor
 - 6 Image Processing Functions
 - 16x16 Grayscale Image
 - Features

- ◆ Status

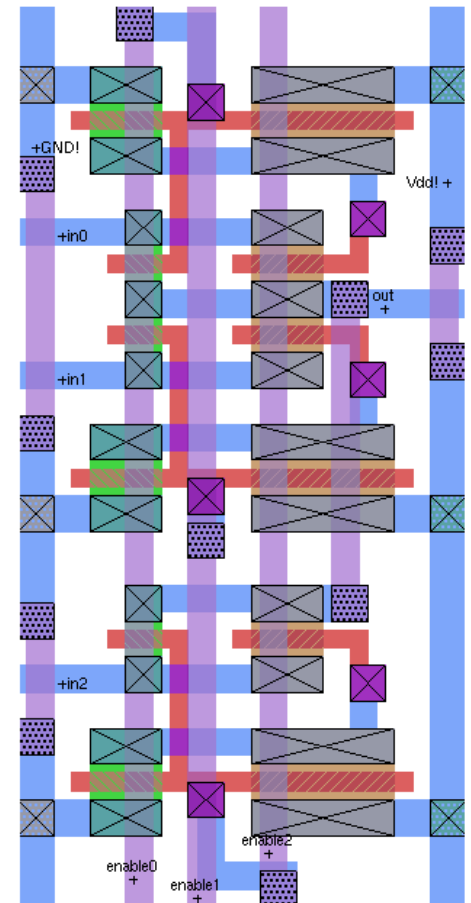
Registers



Muxes

The three input mux (at right) is comprised of three t-gates and three inverters.

The three input muxes are used to regulate the input to register A, while the two input muxes are used on register B and ACC.

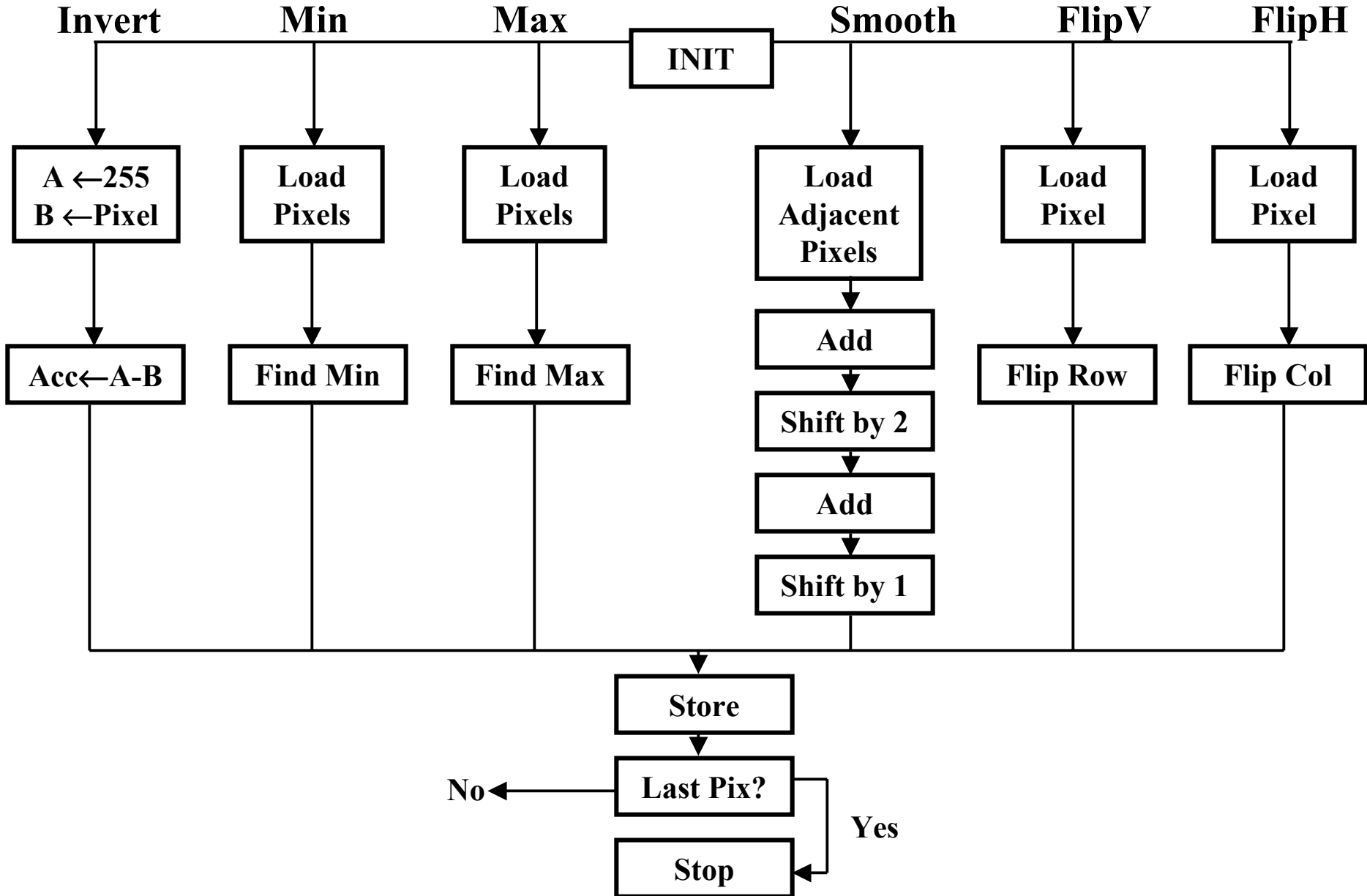


Main Controller Summary

- ◆ ALU Control
 - OpCode
- ◆ Memory Control
 - Read/Write signals
 - Index offset bits
 - Increment
- ◆ Register Control
 - Latch signals
 - Clear signals
 - Enable signals

Function:	Number of State Transitions/Pixel:
Invert	9
Min	31 (worst case)
Max	31 (worst case)
Smoothing	25
Flip Vertical	8
Flip Horizontal	8

Finite State Machine Transitions



Irsim Results for Smoothing



Address Generation Unit

◆ Functions

- Flip Row or Column
- Generate Addresses (Right)

◆ ALU

- Separate 4-bit adders
- Unified 8-bit adder

◆ Separate Memory Controller

- Handshake with Main PLA
- Control Signals

Memory Addresses of Pixels for Min, Max, and Smoothing

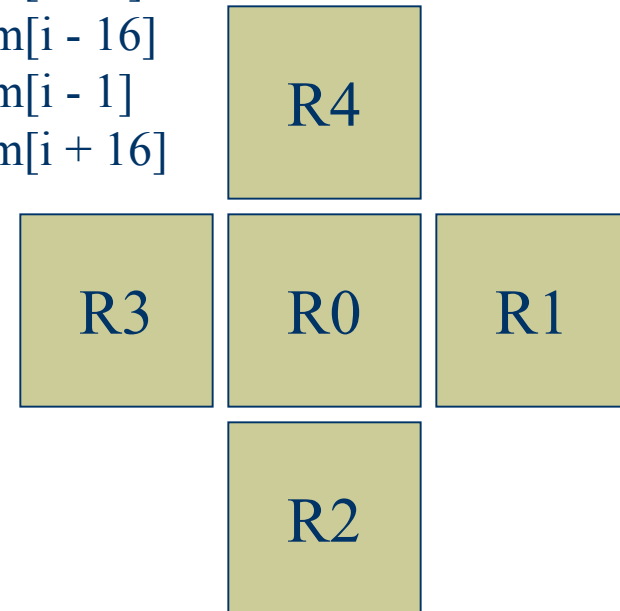
$$R0 = \text{Mem}[i]$$

$$R1 = \text{Mem}[i + 1]$$

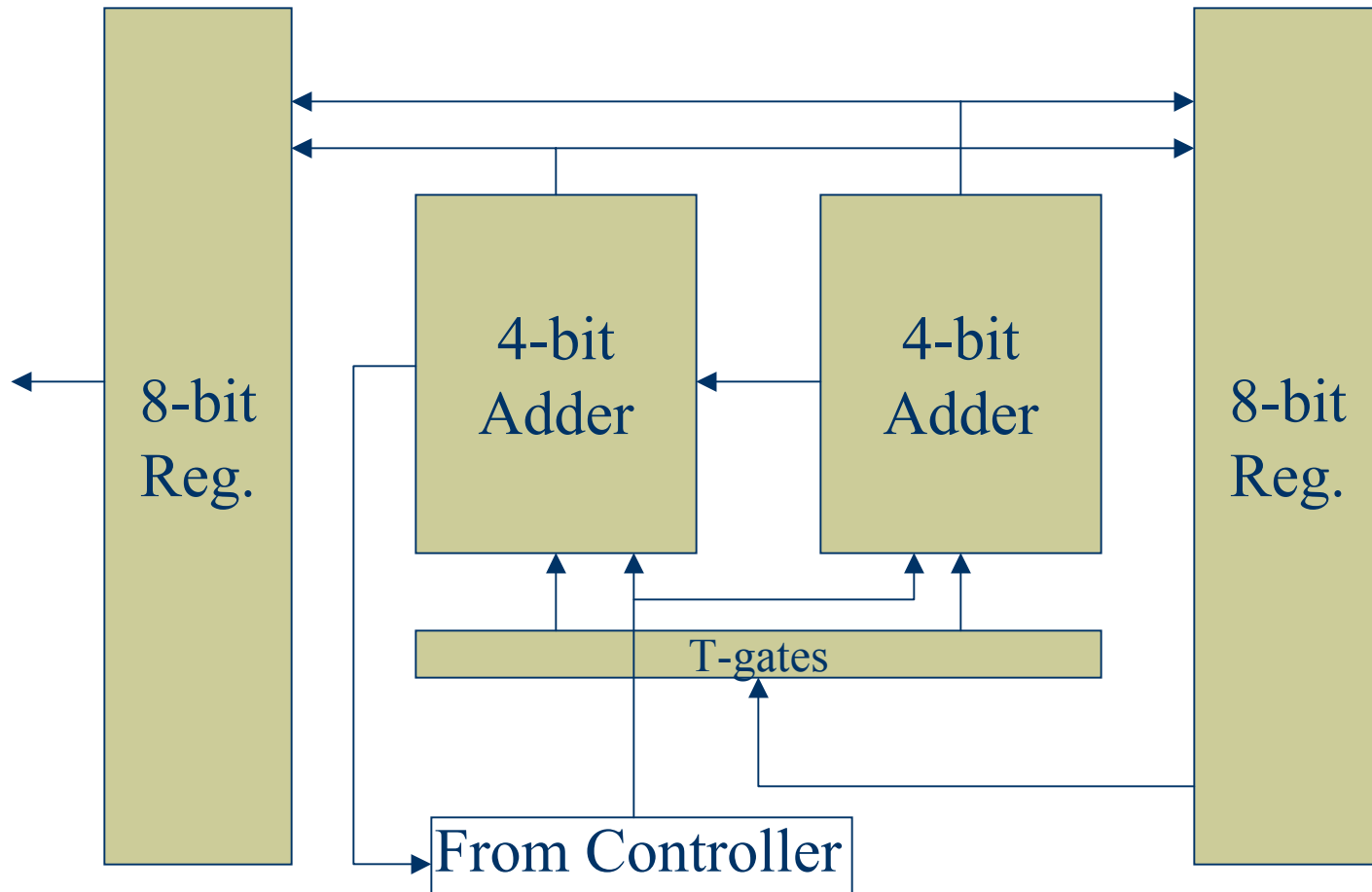
$$R2 = \text{Mem}[i - 16]$$

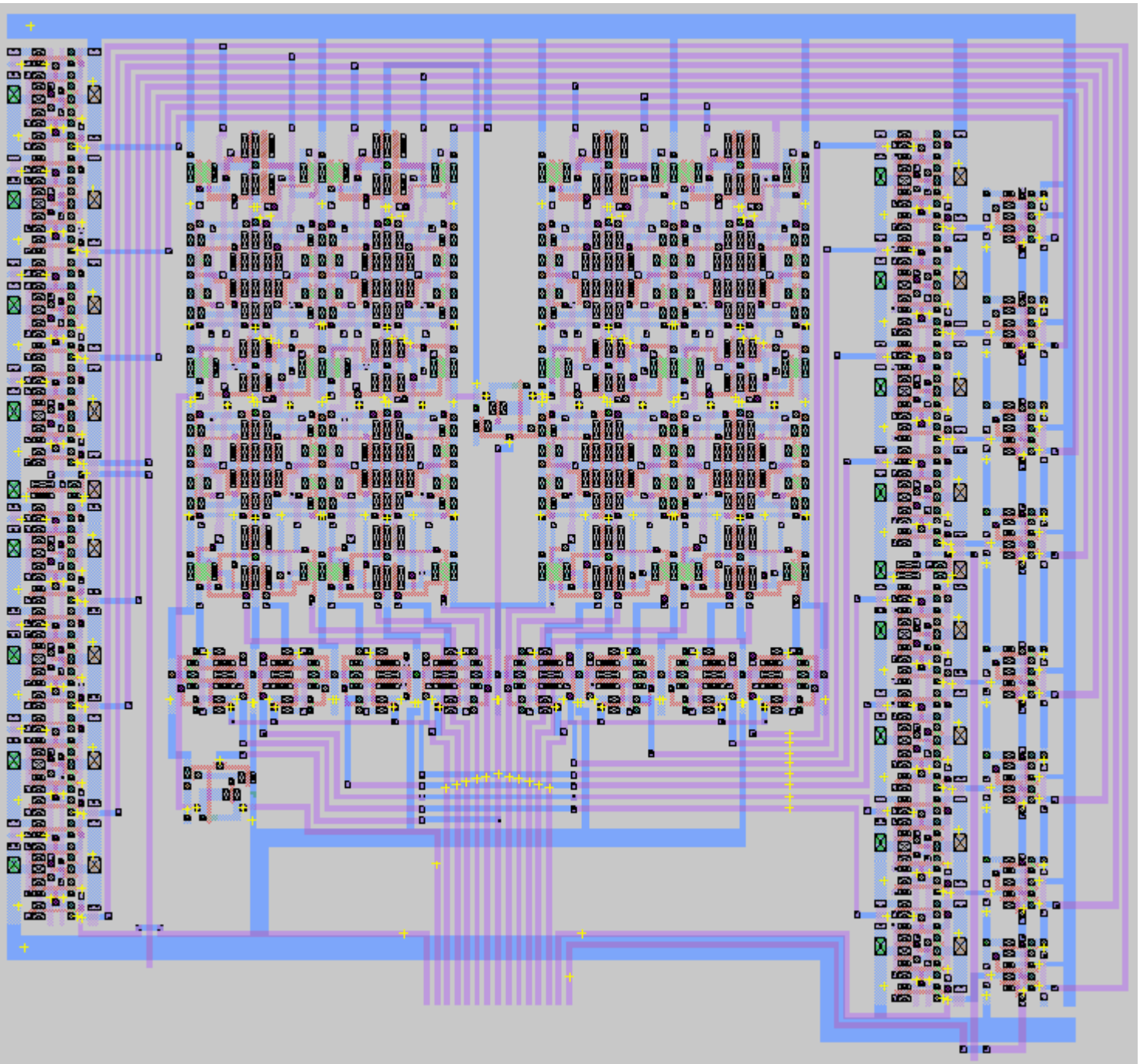
$$R3 = \text{Mem}[i - 1]$$

$$R4 = \text{Mem}[i + 16]$$



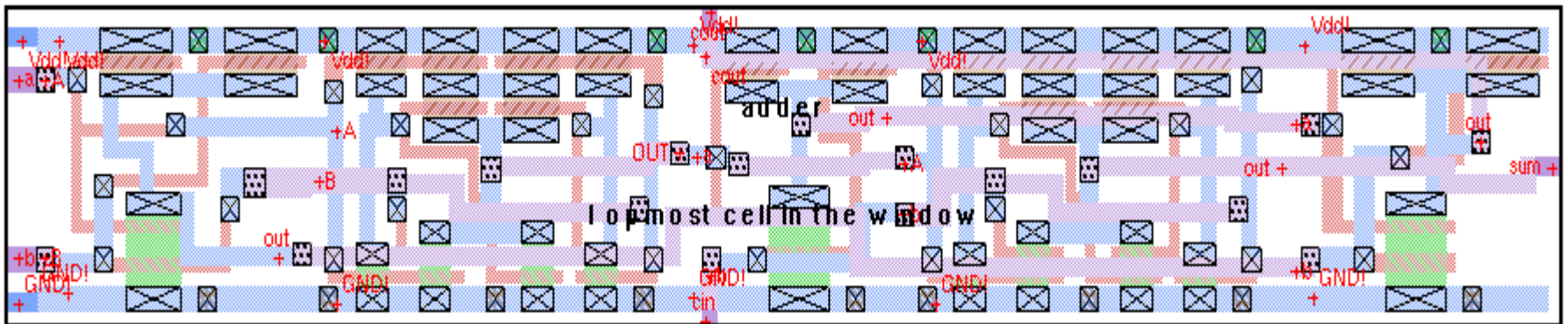
Block Diagram of AGU



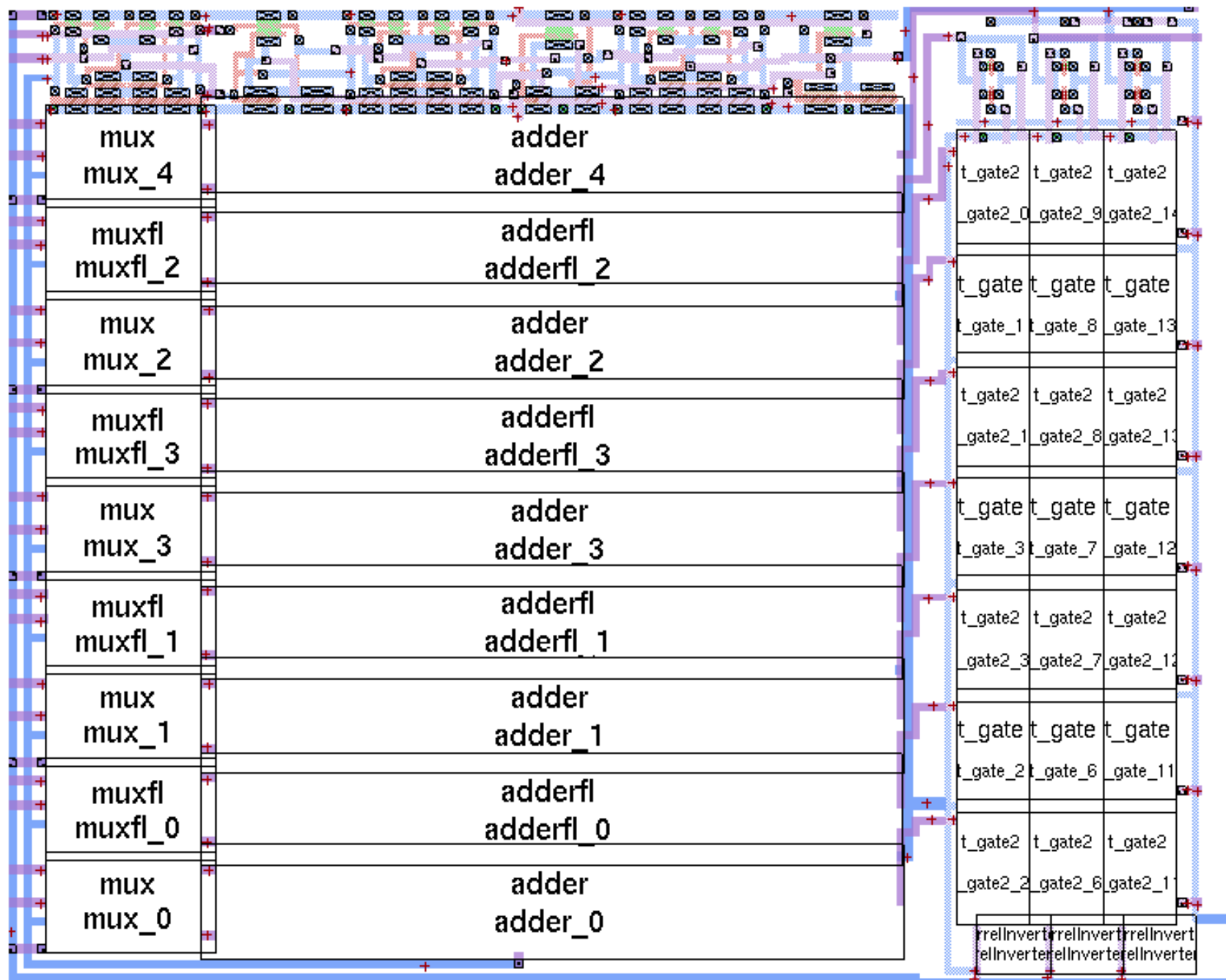


ALU

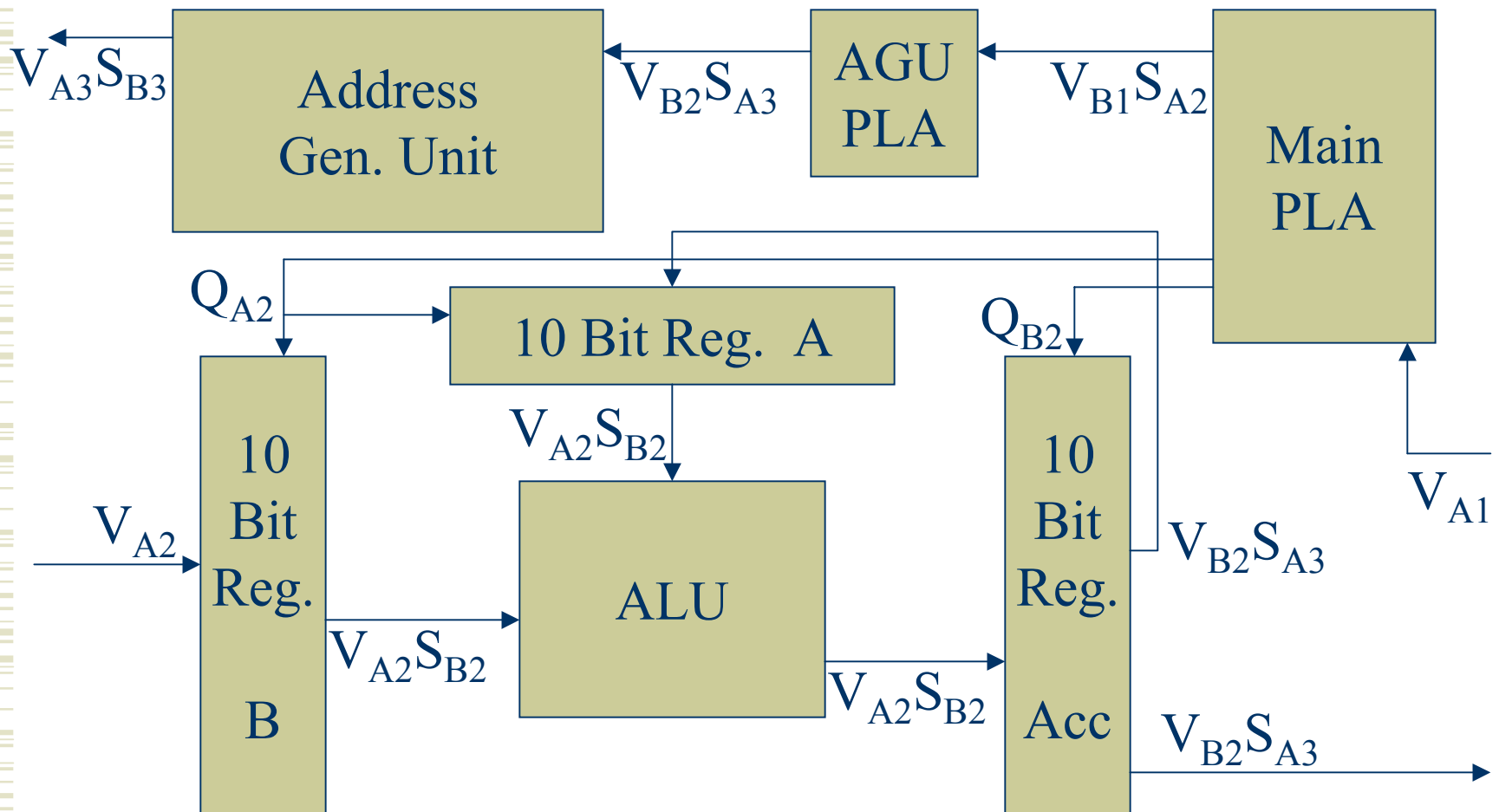
- ◆ 10-bit ripple-carry adder
- ◆ Subtraction
- ◆ Division
- ◆ Comparator



Single Bit Adder Cell



Full System Timing Analysis

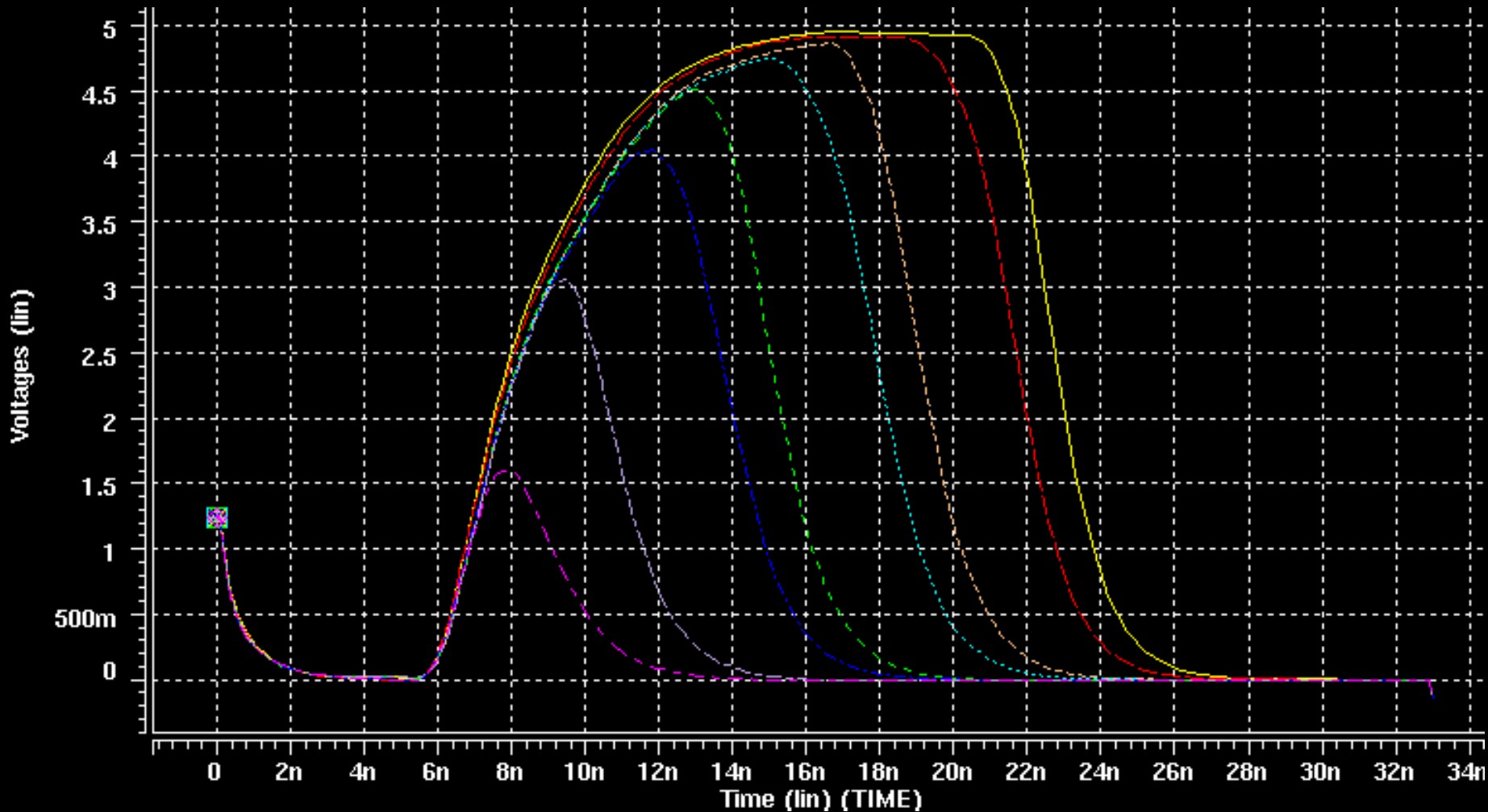


Timing Analysis

Max clock rate: 14 Mhz

Longest Path: 24 ns

R/W access: 70 ns



ALU Spice Analysis

Floorplan

