GP256 Graphics Co-processor

ELEC 422 – VLSI Design I
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Outline

1. Functional Description and Project Status
2. Registers and Multiplexors
3. FSM Controller
4. Address Generation Unit
5. ALU
6. System Performance
7. Floorplan and Cell Hierarchy
Functional Description

- Graphics Co-Processor
  - 6 Image Processing Functions
  - 16x16 Grayscale Image
  - Features

- Status
Registers
Muxes

The three input mux (at right) is comprised of three t-gates and three inverters.

The three input muxes are used to regulate the input to register A, while the two input muxes are used on register B and ACC.
Main Controller Summary

- ALU Control
  - OpCode
- Memory Control
  - Read/Write signals
  - Index offset bits
  - Increment
- Register Control
  - Latch signals
  - Clear signals
  - Enable signals

<table>
<thead>
<tr>
<th>Function</th>
<th>Number of State Transitions/Pixel:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Invert</td>
<td>9</td>
</tr>
<tr>
<td>Min</td>
<td>31 (worst case)</td>
</tr>
<tr>
<td>Max</td>
<td>31 (worst case)</td>
</tr>
<tr>
<td>Smoothing</td>
<td>25</td>
</tr>
<tr>
<td>Flip Vertical</td>
<td>8</td>
</tr>
<tr>
<td>Flip Horizontal</td>
<td>8</td>
</tr>
</tbody>
</table>
Finite State Machine Transitions

- **Invert**
  - A ← 255
  - B ← Pixel
  - Acc ← A - B

- **Min**
  - Load Pixels
  - Find Min

- **Max**
  - Load Pixels
  - Find Max

- **Smooth**
  - Load Adjacent Pixels
  - Add
  - Shift by 2
  - Add
  - Shift by 1

- **FlipV**
  - Load Pixel
  - Flip Row

- **FlipH**
  - Load Pixel
  - Flip Col

- **Store**

- **Last Pix?**
  - No
  - Yes
  - Stop
Irsim Results for Smoothing
Address Generation Unit

- **Functions**
  - Flip Row or Column
  - Generate Addresses (Right)
- **ALU**
  - Separate 4-bit adders
  - Unified 8-bit adder
- **Separate Memory Controller**
  - Handshake with Main PLA
  - Control Signals

**Memory Addresses of Pixels for Min, Max, and Smoothing**

- R0 = Mem[i]
- R1 = Mem[i + 1]
- R2 = Mem[i - 16]
- R3 = Mem[i - 1]
- R4 = Mem[i + 16]
Block Diagram of AGU

8-bit Reg. \(\rightarrow\) 4-bit Adder \(\leftarrow\) T-gates \(\rightarrow\) 4-bit Adder \(\leftarrow\) 8-bit Reg.

From Controller
ALU

- 10-bit ripple-carry adder
- Subtraction
- Division
- Comparator

Single Bit Adder Cell
Full System Timing Analysis

Address Gen. Unit

10 Bit Reg. A

AGU PLA

Main PLA

10 Bit Reg. B

ALU

10 Bit Reg. Acc
Timing Analysis

Max clock rate: 14 Mhz

Longest Path: 24 ns
R/W access: 70 ns