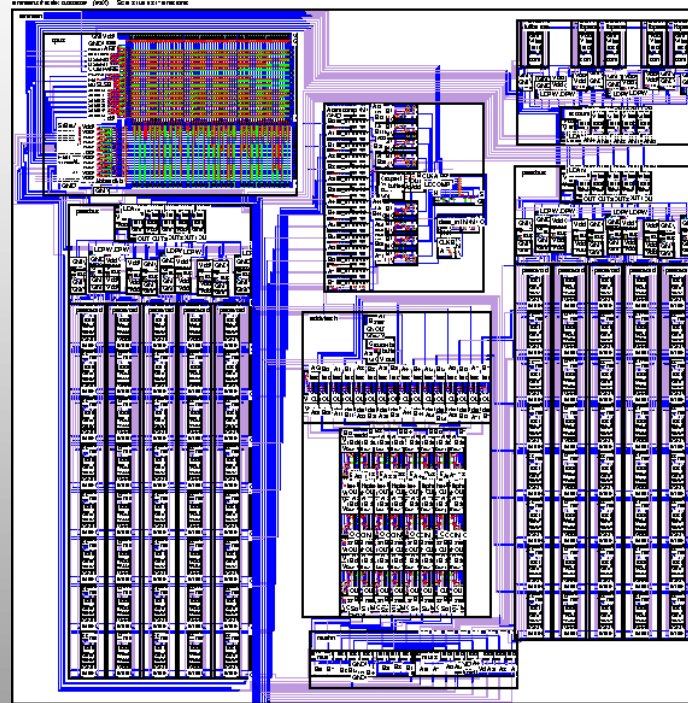


ATM CONTROL



Brian Hill

Jarrold Jensen

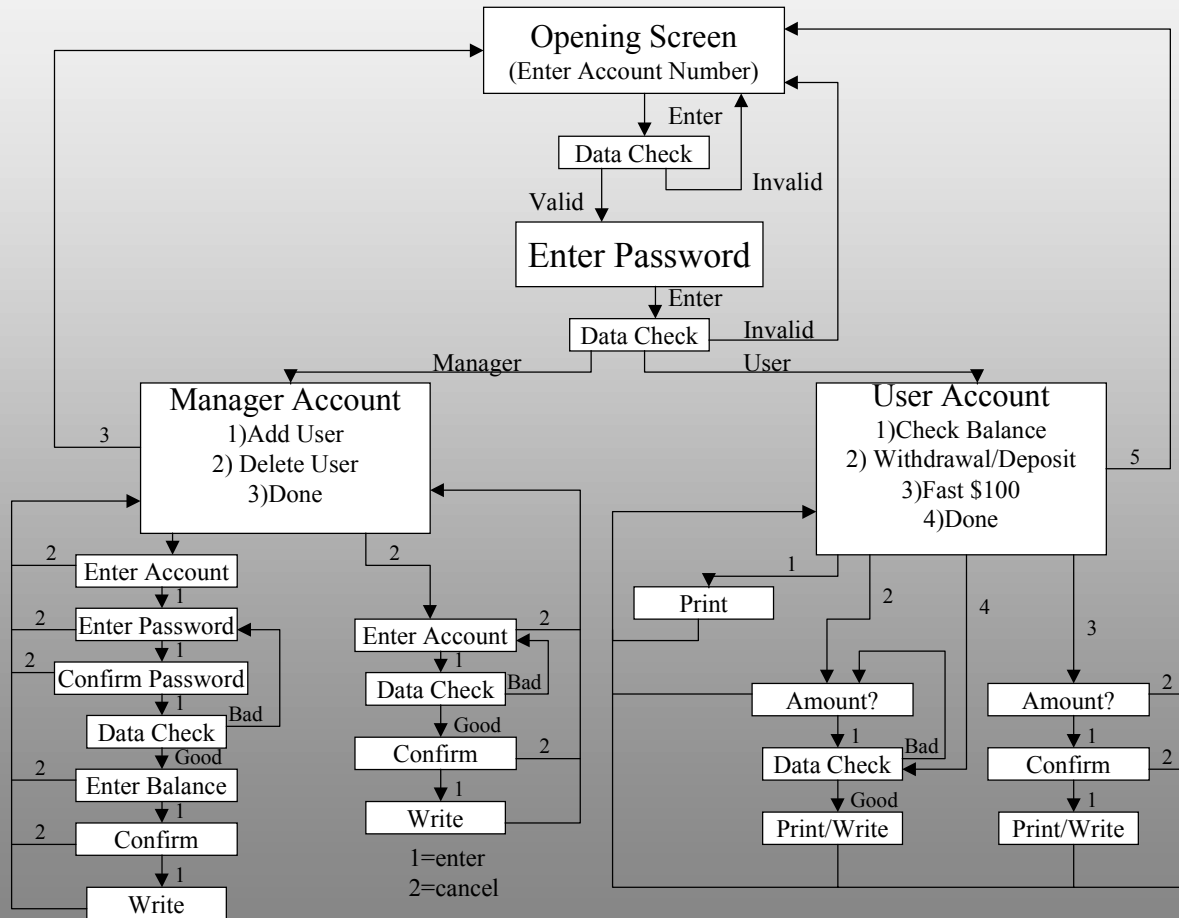
Eric Wingrove

<http://www.owlnet.rice.edu/~jarrod/vlsi>

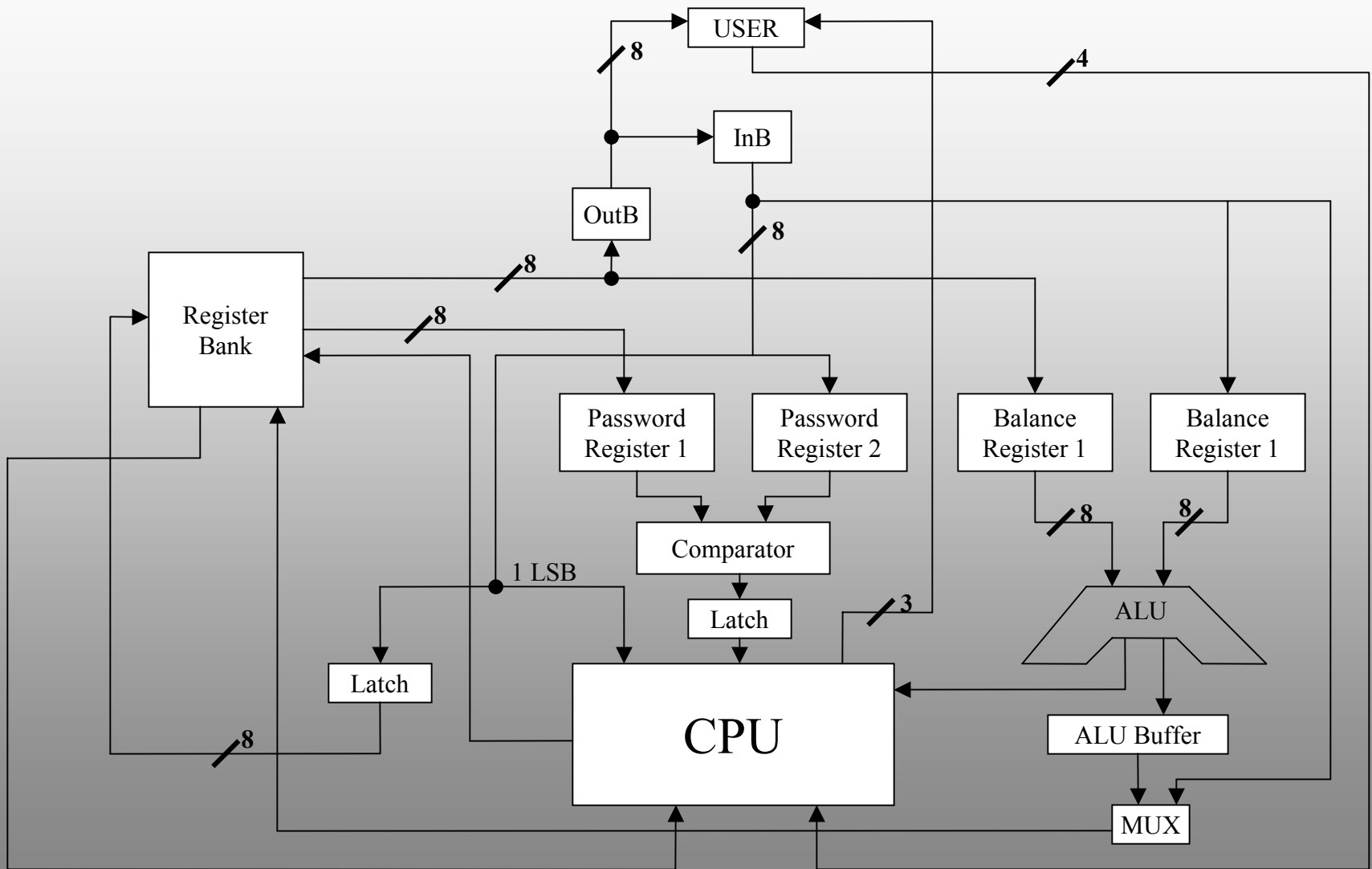
ATM PROCESSOR

- Chip mimics functionality of ATM
- Interfaces with sister group I/O Chip
- Limitations
 - Number of Accounts
 - Balance
 - No permanent storage

Screen Flow Diagram



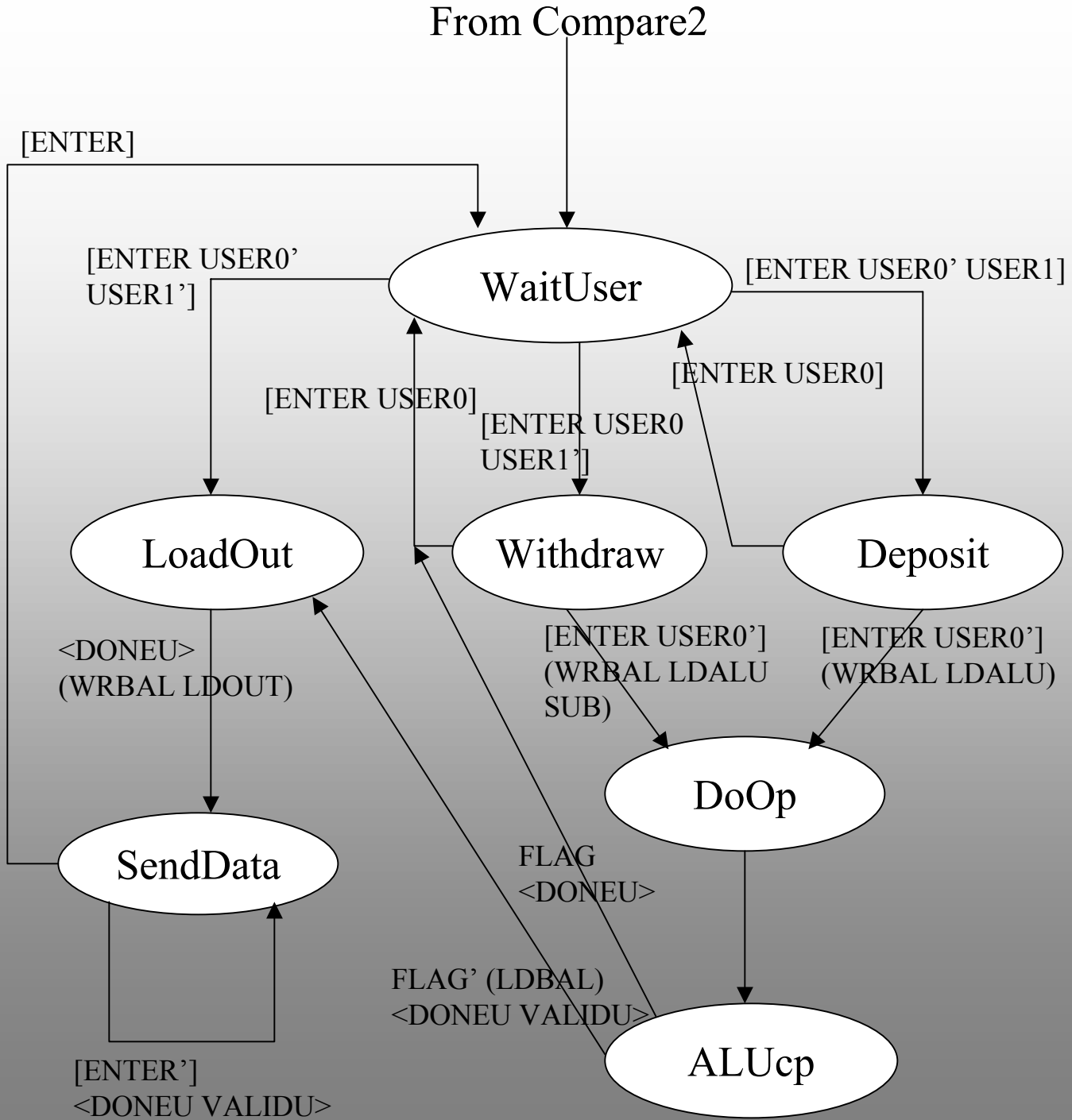
Logic Diagram



System Timing

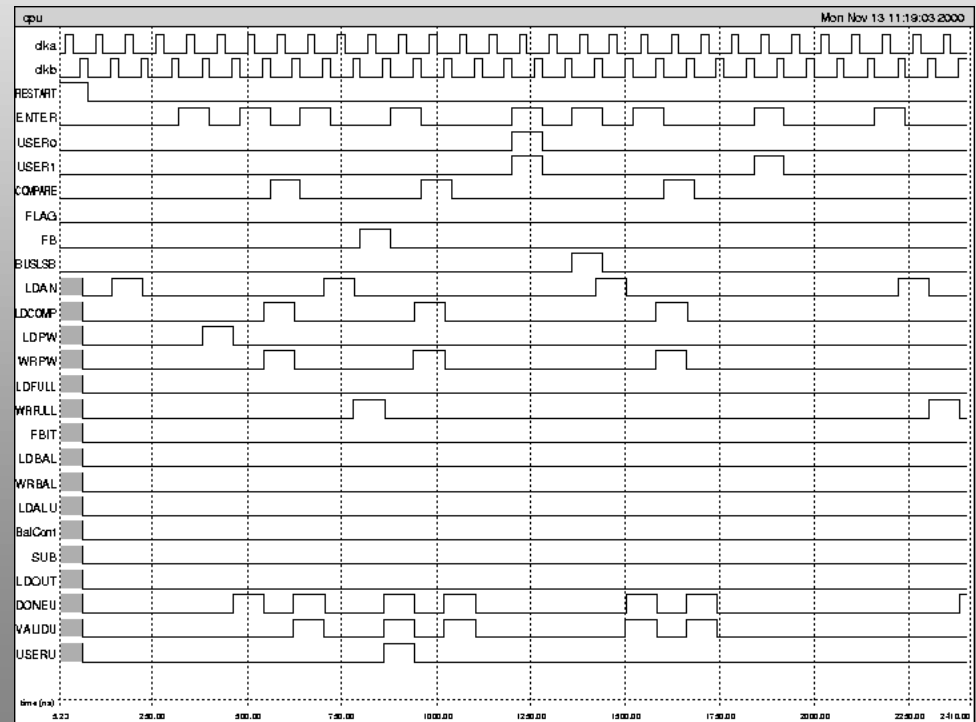
- PLA works with...
 - Adder -latches input on clka and output on clkb
 - extra state to allow for response from adder
 - Comparator
 - same as adder, extra state for comparison bit
 - Register Bank
 - static latches work on clocked control
 - Mux
 - asynchronous control signal

State Diagram

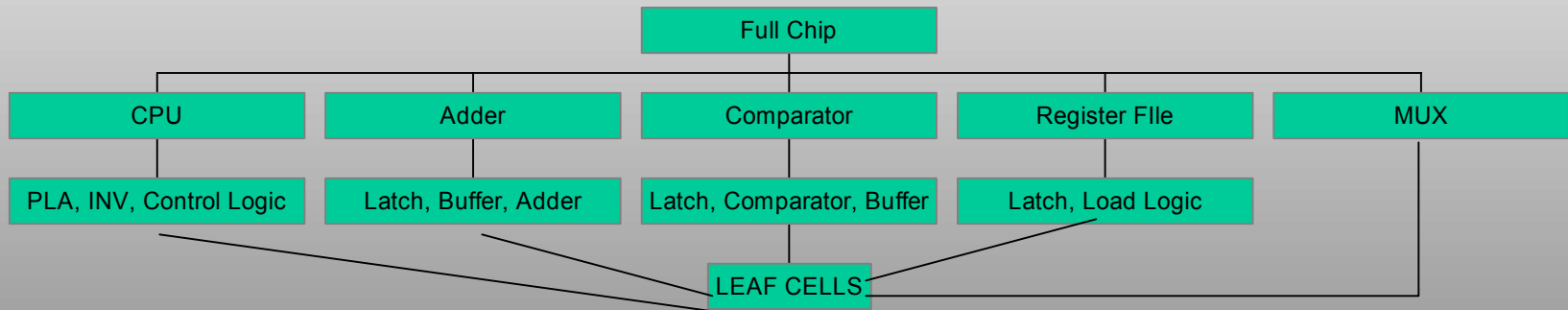


PLA /CPU

- State diagram extension of screen diagram
- Extra states to allow for timing
- Total of 35 states



ATM Cell Hierarchy

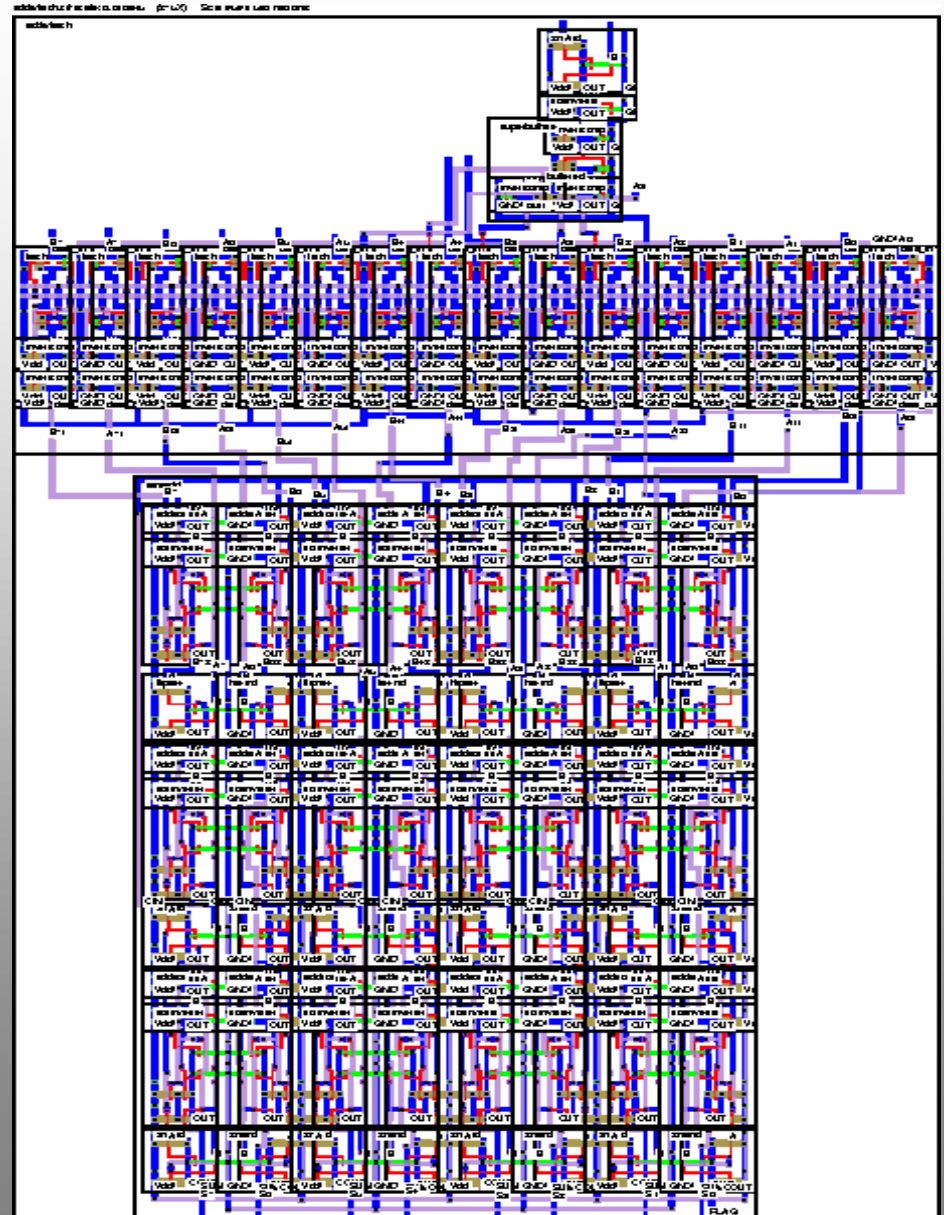


System Performance

- Overall, chip can run at a maximum clock speed of at least 20 MHz
- Crystal slowest path analysis: Adder, Comparator, CPU, full chip
- Spice analysis of those crucial paths
- Limiting component-8 bit ripple carry adder

8-bit Ripple Carry Adder

- Critical path from initial CIN to final COUT
- 48ns for COUT to stabilize when CIN goes low
- Spice simulation confirms this



System Simulation

- Successful simulation of entire chip
 - added a user
 - made a deposit
 - made a withdrawal
 - deleted the user
- I/O pad wiring complete
 - Pad test pending

Final Comments

- Anticipate successful cooperation with sister chip
- Winner required to deposit money using our chip

