CDMA-ish
Pipelined Multi-Stage Multi-User Detector for WCDMA
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Multiuser Detection

- The bits of current, past, and future users overlap
- Algorithm uses correlation matrices to cancel interference due to users' asynchronous transmissions.

\[
y_i^{(l)} = y_i^{(0)} - Ld_i^{(l-1)} - Cd_i^{(l-1)} - Lt d_i^{(l+1)}
\]

\[
d_i^{(l)} = \text{sign}(y_i^{(l)}).
\]
Pipelined Detection

- Pipeline suitable for multiple stages and bit streaming
- Each successive stage improves the bit estimate

![Diagram of Pipelined Detection]

Figure 3: Pipelined Detection. The detection process can be streamlined to work on a bit basis rather than in blocks. As soon as the immediate future bits are available, the next iteration of detection is carried out. Bit 3 is highlighted as an example.
PLA Descriptions

- **MainPLA**: Controls overall synchronization
- **InitPLA**: Reads initial data into storage
- **AddrPLA**: Generates register addresses
- **InputPLA**: Handshakes input independently
- **OutputPLA**: Handshakes output independently
PLA Communication

- Init PLA
  - Valid
  - InitDone
  - StartInit
  - NextAddr
  - MUX
  - InConsumed
  - MUX
  - RowDone

- Main PLA
  - DYOutputOK
  - OutValid

- Input PLA
  - DYInputOK

- Addr PLA
  - MUX

- Output PLA
  - OutConsumed

- MUX
  - IConsumed
  - DYInputOK InConsumed
  - OutConsumed

- MUX
  - DYOutputOK

- MUX
  - OutValid
Make sure previous output happened before generating new output.

\[ \text{Add } d_{i-1} L_{jk} \quad 0 \leq k \leq 4 \]

Make sure input happened

\[ \text{Add } d_i C_{jk} \quad 0 \leq k \leq 4 \]

Ensure input happened

Ensure previous output happened before generating new output.

\[ \text{Add } d_{i+1} L_{jk} \quad 0 \leq k \leq 4 \]

\[ \text{InitPLA turns on} \]

\[ \text{InitPLA turns off} \]

\[ \text{Initialize } L, C, y, d \]

Compute Output Row 1

Compute Output Row 2

Compute Output Row 3

Compute Output Row 4

Compute Output Row 5
Layout - Basic Latch

40x108
Layout - Correlation Matrices

30 x 8 bits
Layout - Adder

440x1220
Critical Subunit - Adder

Worst-case 8.8ns delay through 9 bit adder.
What We Gotz.

- ~475 bits of storage
- 3-bit carry lookahead adder is very fast (8.8ns)
- Conservative estimate of 30 MHz clock allows 400 Kb/sec per user

Metal 3 -->